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Low-power frequency divider in 180 nm CMOS technology for 2.4 GHz phase locked loop applications

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Abstract

This paper presents the design and analysis of a low-power programmable frequency divider implemented in 180 nm CMOS technology, optimized for applications in the 2.4 GHz Bluetooth band. In the proposed architecture, a 32/33 dual-modulus prescaler, a main counter, and a swallow counter are integrated, utilizing true single-phase clock (TSPC) flip flops that enable high-speed operation with minimal power consumption. The design was simulated and evaluated using PSPICE software under a 2V supply voltage, demonstrating stable frequency division with low phase noise. Simulation results revealed a total power consumption of 0.58 mW, with efficient distribution across the prescaler and counter circuits. This work addresses key challenges in power efficiency, operational speed, and circuit area, making it a strong candidate for energy-constrained applications such as Bluetooth transceivers, wireless sensor networks, and IoT devices. With the proposed frequency divider, wireless communications systems can easily integrate PLL-based frequency synthesizers into their next-generation systems. This is a scalable, energy-efficient solution.

Keywords: Programmable Frequency Divider; CMOS Technology; Low-Power Consumption; Phase Locked Loop

1 Introduction

The increasing demand for efficient, low-power circuit designs has driven the rapid evolution of wireless communication systems. Technologies such as Bluetooth, operating within the 2.4 GHz ISM band, play a vital role in IoT, wearable devices, and wireless sensor networks (WSNs). A critical component in such systems is the phase-locked loop (PLL), which ensures frequency stability and synchronization. Within PLLs, programmable frequency dividers are essential for reducing the voltage-controlled oscillator (VCO) frequency to align with a reference signal, enabling precise and stable operation. Advancements in CMOS technology have significantly improved the performance of programmable frequency dividers, balancing trade-offs in power consumption, speed, and area. 2.4 GHz quadrature-input fractional dividers implemented in 0.35 m CMOS achieved efficient operation with just 5.13 mW of power consumption [1]. Using dynamic logic techniques, a high-speed programmable divider demonstrated a power consumption of 3.5 mW for a 2.4 GHz synthesizer [2]. Recent designs, such as an extended true single phase clock (E-TSPC) architecture, have achieved operational frequencies up to 12 GHz with power consumption as low as 1.44 mW, showcasing the scalability of advanced CMOS designs [3]. Wide frequency division ratios and low power are critical for modern GHz-range applications. A dual modulus prescaler, operating at 24 GHz in 65 nm CMOS technology, achieved high phase noise performance [4]. Another design for wireless LAN systems demonstrated ultra-low power consumption and reliable operation at 5 GHz [5]. Similarly, a programmable low-frequency divider implemented in 180 nm CMOS provided exceptional precision and stability across a wide temperature range [6]. Recent advancements have focused on integration and adaptability. A PLL synthesizer for 60 GHz sliding-IF transceivers integrated a programmable divider that supported high precision in millimeter-wave applications [7]. A frequency divider designed using 40 nm CMOS supported a division ratio from 2 to 2048, achieving power consumption of 0.47 mW and meeting

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the demands of IoT applications [8]. For WLAN systems, a low-power divider operating across the 2.4 - 2.48 GHz range with 40 frequency hopping channels consumed just 3.51 mW [9]. Newer designs have addressed challenges such as phase noise and jitter. A wide-band divider for IoT systems achieved robust performance and seamless integration into multi-standard PLLs while maintaining energy efficiency [10]. A 15/16 prescaler design for high-speed PLLs consumed 3.51 mW at 1.8 V and demonstrated efficient reloadable counters for improved adaptability [11]. Additionally, a frequency divider optimized for RTC circuits showed minimal drift across varying supply voltages and temperatures, highlighting its suitability for ultra-low-frequency applications [12]. Phase frequency detectors with charge pumps and programmable dividers have been demonstrated for Bluetooth Low Energy (BLE) operation across 2.4–2.48 GHz. They consume 3.51 mW and use 0.18 μm CMOS technology [13]. A low-power, wide-band programmable divider optimized for IoT and WSN applications highlighted innovations in synchronous counter architectures, achieving minimal power overheads [14]. A high-resolution programmable divider designed using TSPC-based flip-flops provided reliable operation up to 1.8 GHz, consuming just 5.8 mW, showcasing its potential in WLAN systems [15]. Furthermore, an ultra-wide range programmable divider for RTC circuits achieved precise frequency scaling with a minimal jitter effect across varying temperatures and voltages [16]. These advancements emphasize the importance of counter design, prescaler efficiency, and programmability in modern GHz-range wireless applications.

In this paper, design and analysis of a low-power programmable frequency divider implemented in 180 nm CMOS technology is presented. The proposed architecture integrates a 32/33 dual modulus prescaler, a swallow counter and a main counter all optimized for efficient operation within the 2.4 GHz Bluetooth band. Emphasizing power efficiency, high-speed performance, and compact design, this work aims to address key challenges in frequency synthesis, contributing to the development of energy-efficient, high-performance PLL-based synthesizers for next-generation wireless communication systems.

2 CMOS Programmable Frequency Divider

The CMOS programmable frequency divider is a critical component in the feedback path of a phase-locked loop (PLL). It enables precise frequency synthesis by dividing the output frequency of the voltage-controlled oscillator (VCO) [17] according to a programmable division ratio. This functionality is essential for applications such as Bluetooth transceivers operating within the 2.4 GHz ISM band.

The programmable frequency divider is an essential component in the feedback loop of a phase locked loop (PLL). It consists of three primary components: Dual Modulus Prescaler, Swallow Counter and the Main Counter. Typically comprises a dual modulus prescaler with division ratios of P and P+1, along with two programmable down counters: the main counter (M) and the swallow counter (S). Figure 1 illustrates the block diagram of the programmable frequency divider.

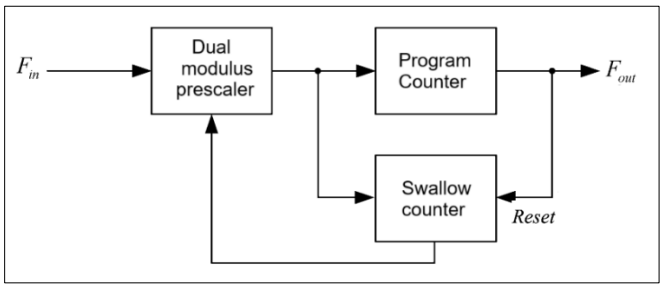

Figure 1 Block diagram of the programmable frequency divider

At the beginning of each cycle, the main and swallow counters are initialized with values M and S, respectively, ensuring that (S ≤ M). The value of S is externally controlled, and both counters decrement with each clock cycle. Initially, the dual modulus prescaler operates with a division ratio of P+1 until the swallow counter reaches zero. Once this occurs, the modulus control signal transitions to a low state, causing the prescaler to switch to a division ratio of P. This continues until the main counter reaches zero, at which point both counters reset, and the process repeats. As a result, the prescaler operates with a division factor of P+1for S cycles and P for (M−S) cycles. This relationship can be mathematically expressed as:

$$N = S(P+1) + (M-S)P = MP + S \quad \ldots\ldots\ldots\ldots \quad (1)$$

Where N is the divider ratio

The relationship between the input and output frequencies of a programmable frequency divider is expressed as:

$$f_{out} = \frac{1}{MP+S} f_{in} = \frac{1}{N} f_{in} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

To determine the appropriate values for P, M, and S, consider a frequency synthesizer operating within the range of 2400 MHz to 2480 MHz, with a reference frequency of 1 MHz. The total division factor, N, which represents the overall division ratio, is calculated as follows:

$$N = \frac{f_{out}}{f_{in}} = \frac{f_{out}}{Channel\ spacing} = 2400 \backsim 2480 \ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

The division ratio of the prescaler can be selected from common values such as 8/9, 16/17, 32/33, or 64/65. In this study, a 32/33 prescaler is chosen. The value of M is determined using the following equation:

$$M = \frac{N}{P} = \left[\frac{2400 \backsim 2480}{32}\right] = 75\ to\ 77 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

The value of S is calculated as follows:

$$S = N - [M \times P] \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

For the given frequency range, S varies from 0 to 16, while M ranges from 75 to 77. However, the design can be easily adapted to accommodate different frequency bands beyond this range, providing flexibility for various communication applications.

2.1 Dual-Modulus Prescaler (32/33)

The prescaler divides the input frequency by either 32 or 33, depending on the modulus control signal. It is constructed using a synchronous divide-by 2/3 circuit combined with an asynchronous divide-by 16 circuit. The architecture employs true single-phase clock (TSPC) D-type flip-flops, ensuring minimal power consumption and high operational speed. Figure 2 shows the block diagram of 32/33 dual-modulus prescaler.

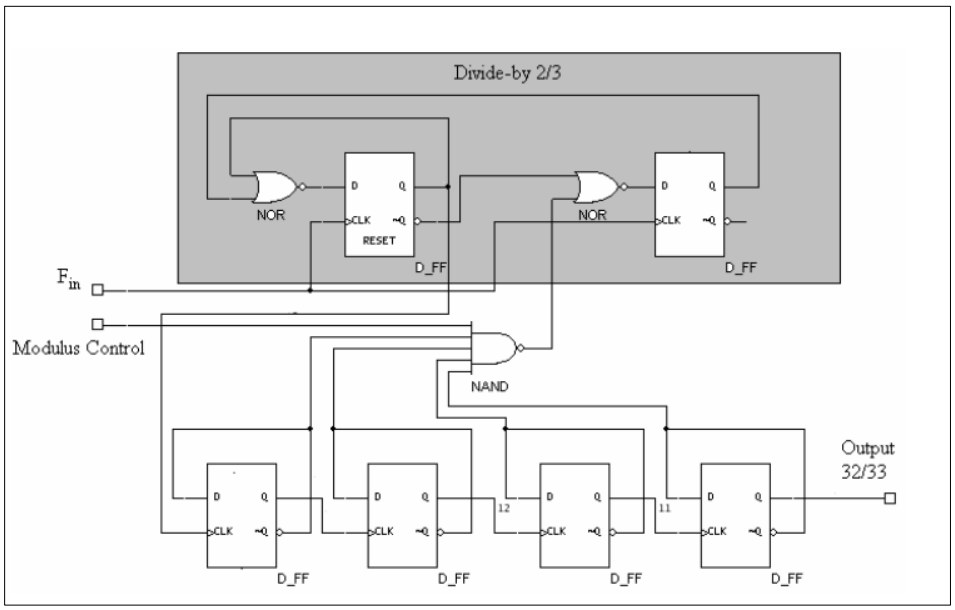

Figure 2 Dual-Modulus Prescaler (divide-by 32/33)

In a dual modulus prescaler, the modulus control signal determines its division ratio. When the modulus control is low, the output of the NAND gate remains high, forcing the divide-by-2/3 circuit to function as a divide-by-2. Consequently, the prescaler operates with a division factor of 32. Conversely, when the modulus control signal is high, the divide-by-

2/3 circuit switches to a divide-by-3 mode, resulting in a prescaler division factor of 33. The dual-modulus prescaler (divide-by-32/33) is designed using a true single-phase clock (TSPC) dynamic D-type flip-flop, as illustrated in Figure 3. The TSPC D flip-flop requires only a single clock phase and consists of nine transistors, reducing circuit complexity and power consumption. Additionally, its minimal propagation delay from D to QB enables high-frequency operation. Due to these advantages, the TSPC-based divider is more efficient and better suited for high-speed applications compared to traditional static dividers.

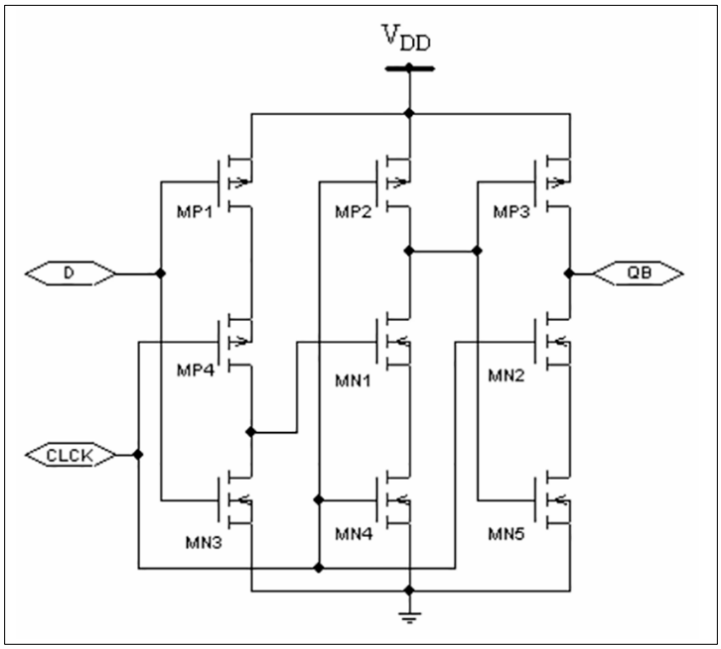

Figure 3 TSPC D-type flip-flop

Dual modulus prescaler operate at the highest frequency with the synchronous divide by 2/3 circuit at the core. As shown in Figure 4, the NOR-based D flip-flop plays a key role in this circuit.

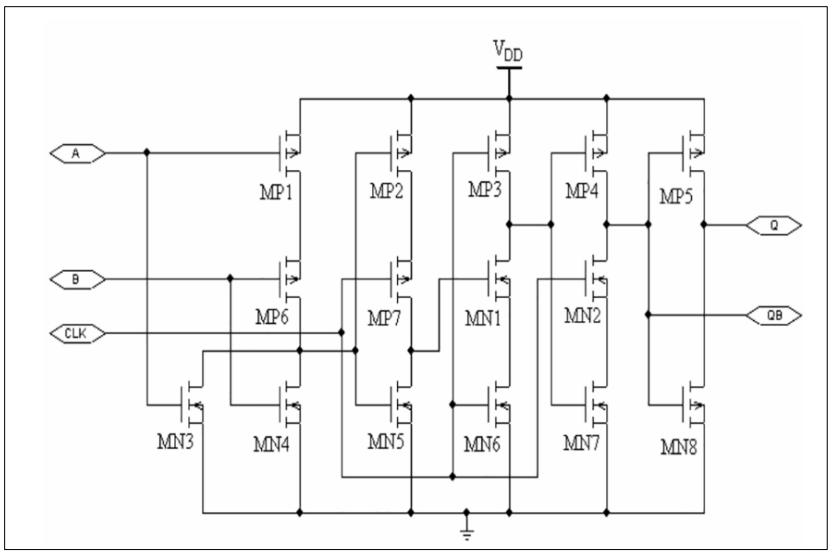

Figure 4 The circuit schematic of NOR/DFF

The divide by 16 asynchronous divider consists of four cascaded divide by 2 stages, as illustrated in Figure 5. Each stage utilizes the same TSPC D flip-flop, ensuring consistent performance and efficient operation. In this configuration, the clock input for each stage is derived from the output of the preceding stage, while the final output is fed back to the D input, enabling sequential frequency division.

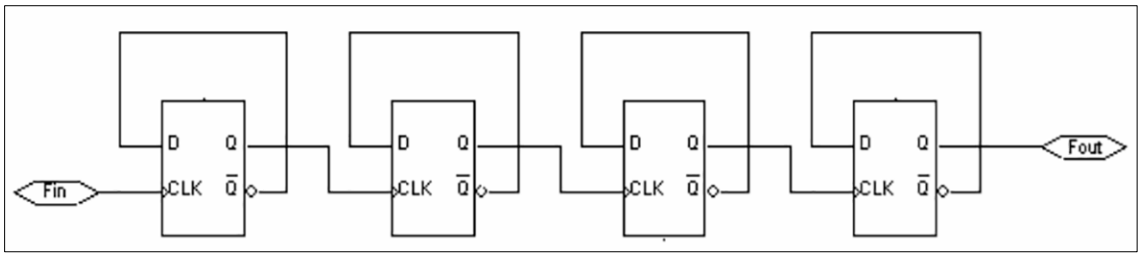

Figure 5 The divide by 16 asynchronous dividers

The dual modulus prescaler was simulated using PSPICE software with a 180 nm CMOS process, operating at a 2V supply voltage. Figure 6 presents the output waveforms for the divide by 32 and divide by 33 modes when subjected to a 4.2 GHz input clock signal.

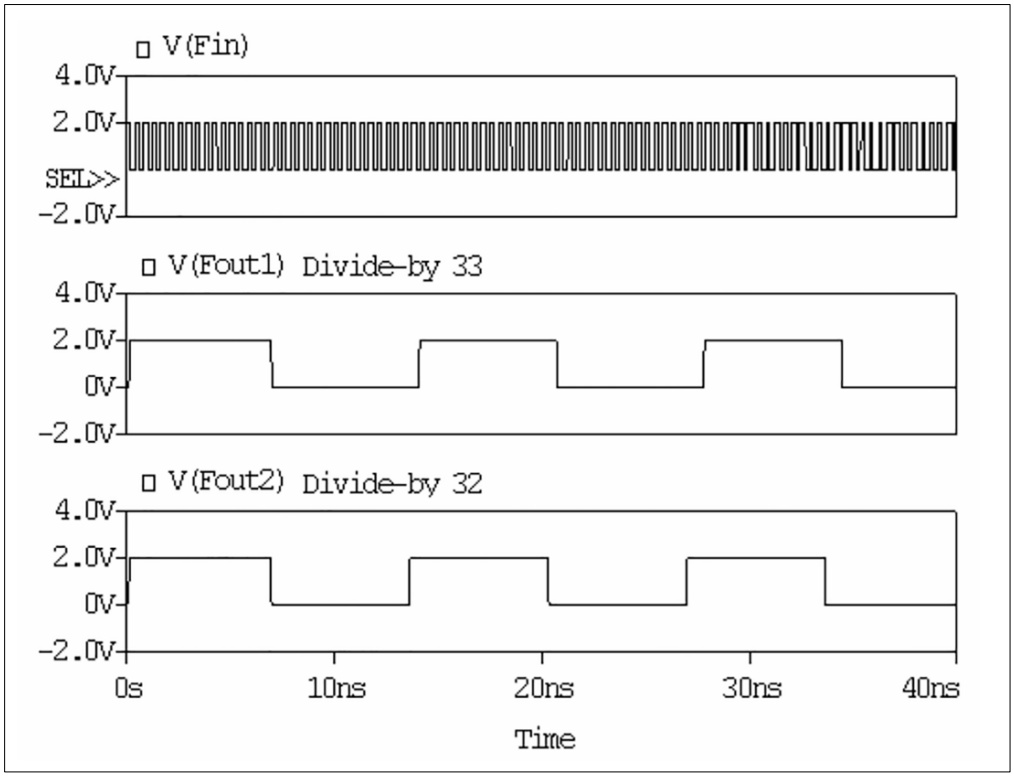

Figure 6 Output waveforms of the dual modulus prescaler divided by 32 and divided by 33.

2.1 Swallow Counter

The swallow counter is a programmable down counter that can be initialized with values ranging from 0 to 16. It works alongside the prescaler to achieve precise control over the division ratio. Designed using TSPC flip-flops, this counter enables the selection of 32 distinct frequency steps, each separated by 1 MHz within the Bluetooth frequency band.

2.2 Main Counter

The main counter is another programmable down counter, initialized with values between 75 and 77, ensuring compatibility with the target frequency range of 2.4–2.48 GHz. Like the swallow counter, it is implemented using TSPC flip-flops, optimizing power efficiency while maintaining high-speed performance.

3 Results and Discussion

CMOS technology 180 nm was used to design the proposed frequency divider, which was evaluated under a 2V supply voltage. The simulation results confirm that the design effectively achieves low-power operation while maintaining

stable high-frequency performance. At 2.4 GHz, the circuit consumes 0.58 mW, divided as follows: 0.245 mW for the dual modulus prescaler and 0.556 mW for the main and swallow counters. TSPC flip-flops plays a significant role in minimizing switching losses while enabling high-speed operation. Compared to conventional frequency divider architectures, this design demonstrates a considerable reduction in power consumption, making it highly suitable for energy-efficient applications.

The simulation results of the divide-by-32 and divide-by-33 modes were obtained using PSPICE, with the corresponding output waveforms confirming stable frequency division with minimal phase noise impact. The effectiveness of the dual modulus prescaler in ensuring accurate frequency scaling is evident in these results. To further assess the efficiency of the proposed divider, a comparative analysis was conducted against other CMOS-based programmable frequency dividers as shown in Table 1. The results indicate that the presented design achieves lower power consumption and improved operational stability compared to designs implemented in 0.35 μm and 65 nm CMOS technologies.

Table 1 Comparison of different prescaler design

Reference	CMOS Technology (nm)	Operating Frequency (GHz)	Power Consumption (mW)	Prescaler Division
[1]	350	2.4	5.13	16/17
[4]	65	24	20	8/9
[9]	180	2.4	3.51	15/16
Proposed	180	2.4	0.58	32/33

The results demonstrate that the proposed frequency divider achieves a power efficiency improvement of over 80% compared to earlier designs while maintaining stable frequency division across the required operating range. Due to its low power consumption and precise frequency control, the programmable frequency divider is well-suited for applications such as Bluetooth transceivers, wireless sensor networks (WSNs), and battery-powered IoT devices. These characteristics ensure extended operational lifespans in portable and energy-sensitive environments. The simulation results validate that the proposed CMOS programmable frequency divider effectively meets the requirements of low-power, high-speed wireless communication systems. The achieved power efficiency, scalability, and reliability make it an ideal candidate for next-generation PLL-based frequency synthesizers. Future research could focus on further reducing leakage power and extending the division range for broader multi-standard applications.

4 Conclusion

This paper presents a low-power programmable frequency divider based on 180 nm CMOS technology for efficient Bluetooth operation at 2.4 GHz. The proposed architecture, comprising a 32/33 dual-modulus prescaler, swallow counter, and a main counter effectively balances power consumption, high-speed performance, and compact design. The design was evaluated using PSPICE simulation software, which enabled comprehensive analysis of the circuit's performance under a 2V supply voltage. The simulation results confirmed stable frequency division with minimal phase noise and demonstrated a total power consumption of 0.58 mW—distributed as 0.245 μW for the dual-modulus prescaler and 0.556 mW for the main and swallow counters. By utilizing True Single-Phase Clock (TSPC) flip-flops, the design achieves significant reductions in switching losses, contributing to enhanced energy efficiency and operational stability. The frequency divider demonstrates strong potential for integration into phase-locked loop (PLL)-based frequency synthesizers, making it highly suitable for modern wireless communication applications such as Bluetooth transceivers, IoT devices, and wireless sensor networks.

Compliance with ethical standards

Disclosure of conflict of interest

No conflict of interest to be disclosed.

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