World Journal of Advanced Engineering Technology and Sciences
eISSN: 2582-8266
Cross Ref DOI: 10.30574/wjaets
Journal homepage: https://wjaets.com/

(RESEARCH ARTICLE)

Check for updates

AI Driven Ultra Low Power VLSI Design Techniques for Wearable and IoT Devices

B. Chandrakala *

Department Of Electronics, Nishitha Degree College, Nizamabad, Telangana, India.

World Journal of Advanced Engineering Technology and Sciences, 2025, 15(03), 2628-2636

Publication history: Received on 19 May 2025; revised on 25 June 2025; accepted on 28 June 2025

Article DOI: https://doi.org/10.30574/wjaets.2025.15.3.1188

Abstract

The rapid proliferation of wearable technologies and Internet of Things (IoT) devices has led to an urgent need for energy-efficient and ultra-low power (ULP) design solutions. These devices often operate in energy-constrained environments, relying on small batteries or energy harvesting sources. This research focuses on the development and optimization of ultra-low power VLSI design techniques to extend battery life and enhance the sustainability of such devices. Key strategies explored include sub-threshold and near-threshold operation, clock and power gating, dynamic voltage and frequency scaling (DVFS), energy-efficient memory architectures, and the integration of non-volatile elements for data retention during power-off states. Moreover, algorithm-level power optimization and AI-assisted design techniques are investigated to tailor computational loads to power budgets dynamically. Special emphasis is placed on hardware-software co-design approaches for wearable biomedical sensors and IoT nodes, ensuring real-time performance under strict power constraints. This work aims to contribute toward the realization of always-on, energy-autonomous systems essential for the next generation of smart, context-aware applications.

Keywords: Ultra Low Power; VLSI Design; AI Hardware; Wearables; IoT Devices; Edge AI; Model Compression; Neural Network Accelerator; In-Memory Computing; Sub-threshold Design

1. Introduction

In recent years, the rapid advancement of technology has driven the widespread adoption of wearable electronics and Internet of Things (IoT) devices across various domains such as healthcare, fitness, environmental monitoring, smart homes, and industrial automation. These devices are characterized by their compact form factor, wireless communication capabilities, and continuous operation requirements. However, one of the most critical challenges in their development and deployment is power consumption. Due to their portable nature, wearables and IoT devices often rely on small batteries or energy harvesting sources, making ultra-low power (ULP) design not only desirable but essential.

Ultra-low power design techniques aim to minimize energy consumption at all levels of the system hierarchy—from the transistor and circuit level up to architecture, system, and software. Unlike traditional power optimization methods, ULP design specifically targets applications where energy resources are severely constrained, and battery replacement or recharging is impractical or impossible. In such scenarios, prolonging battery life or enabling energy-autonomous operation is crucial for ensuring long-term functionality and user convenience.

The design of ultra-low power systems for wearables and IoT involves a multidisciplinary approach that includes:

- Sub-threshold and near-threshold logic design, which reduces voltage levels to minimize dynamic and leakage power.
- Clock gating and power gating, to eliminate unnecessary switching and completely shut off idle blocks.

* Corresponding author: B. Chandrakala

- Dynamic voltage and frequency scaling (DVFS), allowing the system to adjust performance according to workload demand.
- Low-power memory architectures and energy-efficient communication protocols, which are critical for sensor data processing and transmission.
- Non-volatile memory integration and energy harvesting compatibility, enabling intermittent computing and energy reuse.

Additionally, the emergence of machine learning and data-driven applications in edge devices necessitates efficient co-optimization of algorithms and hardware.

This has led to the development of application-specific integrated circuits (ASICs) and systems-on-chip (SoCs) that are specifically tailored for ultra-low power operation. Given the projected growth of IoT and wearable markets, research in ULP VLSI design has gained significant momentum. Innovations in this area directly impact the viability of large-scale deployments and enable the development of smart, always-on, and context-aware systems that align with the vision of ubiquitous computing and sustainable electronics.

The goal of low power design is to reduce the individual components of power as much as possible, thereby reducing the overall power consumption. The power equation contains components for dynamic and static power. Dynamic power is comprised of switching and short-circuit power; whereas static power is comprised of leakage, or current that flows through the transistor when there is no activity. The value of each power component is related to any of the following factors:

- Frequency
- Transition time
- Capacitive load
- Voltage
- Leakage current
- Peak current

For example, the higher the voltage, the higher the power consumed by each component, resulting in higher overall power. Conversely, the lower the voltage, the lower the overall power.

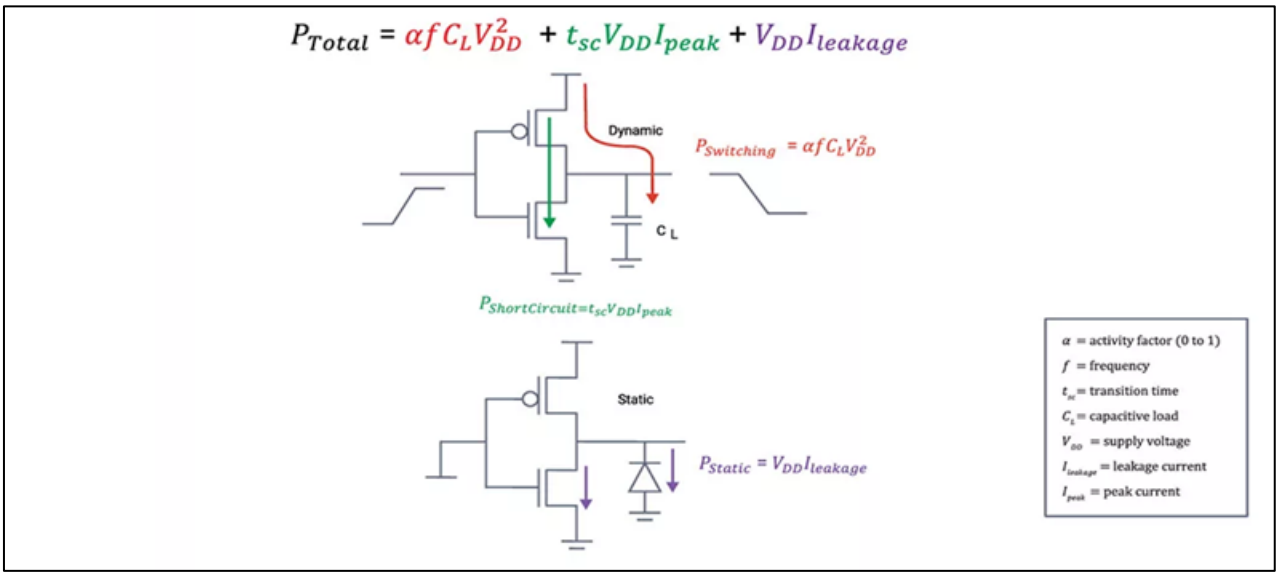

Figure 1 Low Power VLSI Design

This research explores state-of-the-art techniques and proposes novel methodologies for ultra-low power design in wearable and IoT applications, aiming to bridge the gap between performance and energy efficiency.

2. Literature review

The demand for compact, energy-efficient systems has led to significant research in the field of ultra-low power (ULP) VLSI design, particularly for wearable and IoT devices, which operate under strict power and area constraints. This literature review surveys recent developments and trends in ULP design at various abstraction levels, including circuit, architectural, and system-level techniques, and highlights gaps that this research aims to address.

2.1. Sub-threshold and Near-threshold Logic Design

Sub-threshold logic operates transistors below their threshold voltage, reducing dynamic and leakage power significantly. Chandrakasan et al. (2005) and Calhoun et al. (2010) demonstrated that sub-threshold circuits are ideal for ultra-low energy operations, though they face challenges in variability, noise margins, and reduced performance. Near-threshold designs offer a compromise between energy efficiency and reliability. Researchers such as Wang et al. (2012) have proposed adaptive body biasing and error-tolerant logic to improve yield in such environments.

2.2. Clock and Power Gating Techniques

Clock gating reduces dynamic power by disabling the clock signal to inactive modules, while power gating cuts off power supply to idle blocks to eliminate leakage power. Benini and Micheli (2002) presented early models of power gating in mobile systems, and more recently, Kumar et al. (2018) introduced fine-grained power gating controllers for wearables that dynamically respond to context changes. These techniques are widely integrated into commercial low-power SoCs such as ARM Cortex-M series.

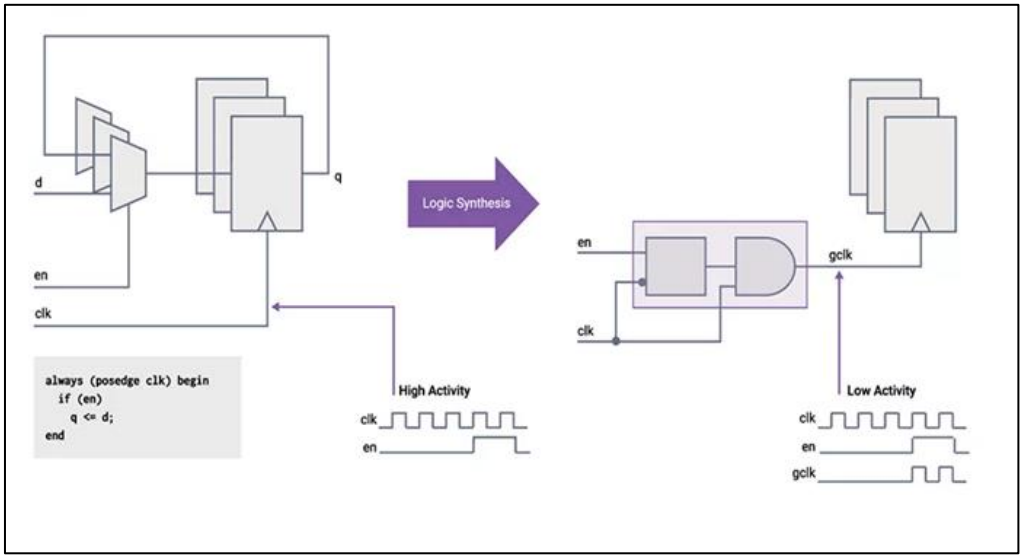

Figure 2 Clock Gating

2.3. Dynamic Voltage and Frequency Scaling (DVFS)

DVFS adjusts voltage and frequency based on workload, balancing performance and power. Kim et al. (2015) developed hardware-software DVFS frameworks that leverage real-time task scheduling. In wearable devices, real-time responsiveness is key; therefore, Liu et al. (2019) proposed lightweight DVFS schemes integrated with workload prediction models for health-monitoring sensors.

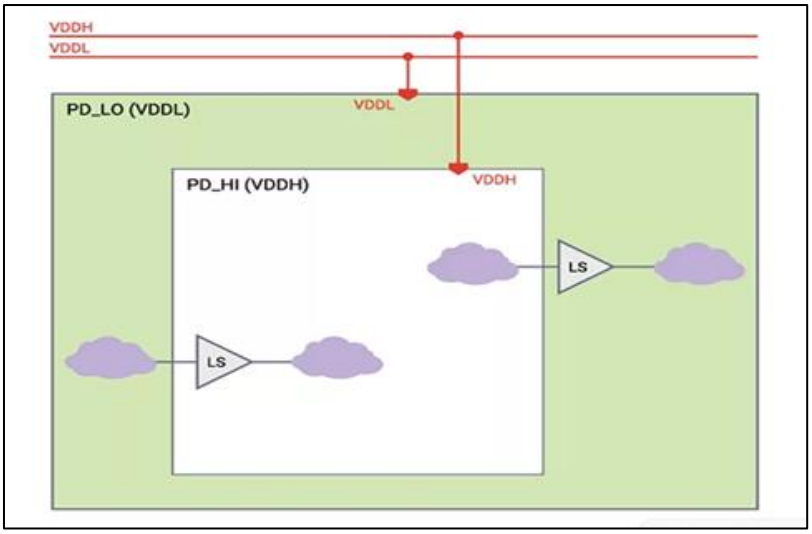

Figure 3 Dynamic Voltage

2.4. Energy-Efficient Memory and Data Handling

Memory is a critical power bottleneck. Researchers have explored multi-bank memory architectures, non-volatile memories (NVMs) like FRAM and MRAM, and approximate computing in memory operations. Alioto (2017) provided a comprehensive survey of low-power memory design, especially in the context of intermittent computing in IoT nodes.

2.5. Energy Harvesting and Power Management

Energy harvesting enables autonomous operation of IoT nodes. Dey et al. (2020) discussed hybrid energy harvesting circuits and energy-aware power management units (PMUs) that adapt to input fluctuations. Coupling PMUs with non-volatile processors (NVPs) has proven effective in extending uptime during low ambient energy periods.

2.6. Application-Specific Architectures for AI and Sensing

The need for local data processing in edge devices has spurred interest in AI accelerators optimized for ULP. Chen et al. (2020) introduced Eyeriss, a reconfigurable CNN accelerator with power gating and data reuse mechanisms. Similarly, Jain et al. (2021) proposed ULP reconfigurable cores for biomedical signal processing using compressive sensing and low-bit quantization.

2.7. Hardware-Software Co-Design and Emerging Trends

Modern design methodologies favour co-optimization between hardware and software to achieve application-level power savings. Recent studies focus on using machine learning for design space exploration, such as reinforcement learning for dynamic power management (Huang et al., 2022). Also, the trend of integrating flexible electronics and ultra-low power wireless communication like BLE 5.0 and LoRaWAN supports new design paradigms.

2.8. Research Gaps Identified

- Need for unified frameworks that combine sub-threshold operation with adaptive power management and energy harvesting.
- Lack of modular design methodologies that allow reusability of ULP IPs across heterogeneous IoT platforms.
- Insufficient attention to ultra-low power AI/ML model integration in resource-constrained wearable environments.

3. Problem statement

The exponential growth of wearable and IoT (Internet of Things) devices has created an increasing demand for ultra-low power (ULP) VLSI design solutions to meet the stringent energy constraints of these platforms. These devices are expected to operate continuously, often on limited power sources such as small batteries or ambient energy harvested from the environment. Despite advancements in low power design techniques at various abstraction levels (device,

circuit, architecture, and system), there remains a significant gap in developing holistic, scalable, and application-specific ULP design frameworks that ensure energy efficiency without compromising performance or reliability.

Most existing techniques either focus on isolated layers (e.g., only circuit-level optimizations) or are not optimized for real-time, context-aware wearable and IoT scenarios. Moreover, integrating AI and machine learning in edge devices further complicates the power-performance trade-offs. Therefore, there is a critical need for new design methodologies that incorporate adaptive, intelligent, and cross-layer strategies to achieve sustainable ultra-low power operation in heterogeneous and dynamic environments.

4. Objectives

The primary objective of this research is to develop and evaluate ultra-low power (ULP) VLSI design techniques. The specific objectives are as follows:

- **To analyse and benchmark existing ultra-low power design techniques**
  Evaluate state-of-the-art low power strategies at various abstraction levels (circuit, architecture, and system) relevant to wearable and IOT devices.
- **To design energy-efficient circuits using sub-threshold and near-threshold logic**
  Investigate the trade-offs between power, performance, and reliability when operating at ultra-low voltages, and propose improved techniques for variability mitigation.
- **To develop dynamic power management schemes**
  Implement and optimize techniques such as clock gating, power gating, and dynamic voltage and frequency scaling (DVFS) to reduce both dynamic and static power in real-time applications.
- **To integrate energy harvesting and power-aware control mechanisms**
  Design power management units (PMUs) that interface with energy harvesting modules, enabling energy-autonomous operation of IOT and wearable platforms.
- **To explore the use of non-volatile memory and intermittent computing**
  Incorporate NVM technologies (e.g., FRAM, MRAM) to support energy retention and seamless recovery during power loss, especially in energy-harvesting scenarios.
- **To propose AI- and ML-assisted power optimization models**
  Apply lightweight machine learning models to predict workload and dynamically adapt power states, enhancing system-level energy efficiency without affecting performance.
- **To develop a hardware-software co-design framework**
  Create a unified framework that supports application-specific customization and enables co-optimization of algorithms and hardware for ultra-low power operation.
- **To validate the proposed techniques through simulation and prototyping**
  Implement the proposed techniques in simulation environments (e.g., Cadence, Synopsys, or FPGA platforms) and evaluate them using real-world IoT and wearable case studies (e.g., health monitoring, motion sensing).

5. Scope of the study

The scope of this research encompasses the exploration, development, and validation of ultra-low power (ULP) design techniques specifically targeted at wearable and Internet of Things (IoT) devices, which operate under limited power budgets and strict size and performance constraints.

This study focuses on the following key areas:

- **Device and Circuit-Level Optimization**

Investigating low-power circuit design methodologies such as sub-threshold and near-threshold operation, leakage reduction, and transistor sizing, which are critical for energy-constrained environments.

- **Architectural and System-Level Techniques**

Exploring architectural strategies including power gating, clock gating, and dynamic voltage and frequency scaling (DVFS) to reduce both static and dynamic power consumption.

- **Energy Harvesting and Power Management**

Designing interfaces for integrating energy harvesting modules (solar, thermal, RF, etc.) and developing intelligent power management units (PMUs) to support intermittent and energy-autonomous operation.

- **Non-Volatile and Energy-Retentive Memory Integration**

Implementing memory architectures that utilize non-volatile memory technologies (e.g., MRAM, FRAM) to ensure data retention during power losses and enable intermittent computing.

- **Hardware-Software Co-Design**

Creating a unified co-design approach to optimize power consumption through collaboration between hardware configurations and software algorithms tailored for wearable and IoT applications.

- **Application-Specific Use Cases**

Focusing on real-world applications such as wearable health monitoring, fitness tracking, environmental sensing, and smart home IoT nodes, to evaluate and validate the practicality of the proposed techniques.

- **Simulation and Prototype Validation**

Utilizing industry-standard EDA tools (e.g., Cadence, Synopsys) for VLSI design simulation and prototyping on FPGA or ASIC platforms to assess energy efficiency, performance, and reliability metrics.

Limitations

- The study primarily focuses on digital design techniques; analog low-power design is outside the core scope.
- Power optimization for large-scale IoT cloud infrastructure is not covered.
- Environmental and manufacturing variations are considered only within typical process variation models.

6. Proposed methodology

The proposed methodology aims to develop, implement, and evaluate comprehensive ultra-low power (ULP) VLSI design techniques for wearable and IoT (Internet of Things) devices. The approach integrates circuit-level optimizations, architectural enhancements, power management strategies, and hardware-software co-design frameworks. The methodology is divided into the following key phases:

6.1. Phase 1: Requirement Analysis and Literature Survey

6.1.1. Objectives:

- Identify and classify the power consumption characteristics of wearable and IoT applications.
- Conduct a detailed literature review of existing ULP techniques at various design abstraction levels.
- Analyse energy profiles and usage patterns of typical wearable and IoT devices (e.g., health monitors, smart sensors, BLE beacons).

6.1.2. Activities:

- Selection of representative target applications (e.g., biomedical wearables, environmental IoT sensors).
- Define application constraints: power budget, area, performance, and latency.
- Benchmark existing ULP designs for comparative analysis.

6.2. Phase 2: Circuit-Level Ultra-Low Power Design

6.2.1. Objectives

- Design digital building blocks (logic gates, flip-flops, ALUs, memory) that operate reliably in sub-threshold and near-threshold voltage ranges.
- Address process variation, timing uncertainty, and leakage power.

6.2.2. Techniques to be used:

- **Sub-threshold Logic Design:** Operate CMOS logic below V_{th} to minimize dynamic power.
- **Body Biasing and Adaptive Threshold Techniques:** For leakage mitigation.
- **Minimum Energy Point (MEP) Identification:** To determine the optimal operating voltage for energy efficiency.

6.2.3. Tools

- Cadence Virtuoso for schematic and layout.
- HSPICE/Spectre for transistor-level simulations.

6.3. Phase 3: Architectural-Level Power Management

6.3.1. Objectives

- Implement and optimize system-level strategies such as clock gating, power gating, and dynamic voltage and frequency scaling (DVFS).
- Enable selective activation/deactivation of functional blocks based on workload.

6.3.2. Techniques to be used

- **Fine-grained Clock Gating**: Integrate at the module and register-transfer level.
- **Multi-threshold CMOS (MTCMOS) and Power Gating**: Design power switch cells and retention flip-flops.
- **DVFS Implementation**: Introduce multiple voltage/frequency islands.

6.3.3. Tools

- Synopsys Design Compiler and Power Compiler for RTL synthesis and power analysis.
- UPF/CPF (Unified/ Common Power Format) for power intent modelling.

6.4. Phase 4: Energy Harvesting and Power Management Integration

6.4.1. Objectives

- Design and simulate energy harvesting circuits and power management units (PMUs).
- Enable intermittent computing and energy-autonomous operation.

6.4.2. Activities

- Design energy buffers, voltage regulators, and charge management units compatible with solar, piezoelectric, or RF sources.
- Implement check pointing mechanisms using non-volatile memory to store processor states during power loss.

6.4.3. Tools

- MATLAB/Simulink for system modelling.
- Cadence AMS Designer for mixed-signal simulation.

6.5. Phase 5: Hardware-Software Co-Design and AI-Driven Adaptation

6.5.1. Objectives

- Co-optimize firmware and low-level algorithms for reduced power consumption.
- Use machine learning (ML) for dynamic power-state prediction and workload classification.

6.5.2. Activities

- Develop lightweight ML models (e.g., decision trees, reinforcement learning) to control DVFS and power gating based on sensor activity and application context.
- Embed firmware routines for real-time energy-aware task scheduling and peripheral control.

6.5.3. Tools

- Embedded C and Python for firmware and ML model development.
- RISC-V/ARM Cortex-M platforms for testing.

6.6. Phase 6: Prototyping and Experimental Validation

6.6.1. Objectives

- Validate the proposed design techniques using FPGA or ASIC platforms.
- Measure real-time power consumption, latency, and reliability.

6.6.2. Activities

- Implement selected modules on FPGA (Xilinx/Intel) using ultra-low power IP cores.
- Develop a test bench for typical IoT workloads.
- Use digital multimeters, logic analysers, and power meters for power profiling.

6.6.3. Metrics for Evaluation

- Average and peak power consumption.
- Energy per operation (EPO) and Energy per inference (for AI-based designs).
- Latency, area, and throughput.
- Battery life extension ratio (compared to baseline design).

6.7. Phase 7: Case Studies and Application Validation

6.7.1. Objectives

- Deploy the complete design on representative wearable and IoT devices.
- Validate performance in real-world scenarios.

6.7.2. Use Cases

- **Wearable Health Monitor**: ECG or PPG-based heart rate tracking system.
- **IoT Environmental Node**: Air quality or temperature monitoring with BLE/Lora transmission.

6.7.3. Evaluation Criteria

- End-to-end energy profiling.
- Real-time responsiveness and data retention during power loss.
- Compliance with industry power benchmarks (e.g., <10 μW standby).

7. Expected outcomes

The research is expected to contribute significantly to the field of energy-efficient VLSI systems through novel, scalable, and application-specific solutions. The major expected outcomes are as follows:

- Development of Energy-Efficient Building Blocks
  - Design and validation of ultra-low power digital logic components operating in sub-threshold and near-threshold voltage regimes, optimized for wearable and IoT applications.
  - Demonstration of reliable performance under process variations and low voltage conditions.
- Enhanced Power Management Strategies
  - Implementation of fine-grained clock gating, power gating, and DVFS techniques customized for real-time, context-aware applications.
  - Demonstrated reduction in both dynamic and static power consumption across different workloads.
- Integration of Energy Harvesting and Power Autonomy
  - Realization of intelligent power management units (PMUs) that interface with energy harvesting sources (e.g., solar, thermal, RF), enabling battery-less or extended-operation devices.
  - Support for intermittent computing using check pointing and non-volatile memory integration.
- AI-Enabled Runtime Power Optimization

  - Introduction of lightweight machine learning models for runtime workload prediction and adaptive power state management.
  - Reduction in energy per operation through predictive, autonomous power control strategies.
- Hardware-Software Co-Design Framework
  - A reusable and scalable co-design framework enabling application-specific customization for a variety of IoT and wearable use cases.
  - Demonstration of improved energy efficiency and system performance compared to conventional designs.
- Prototype Demonstration and Real-World Validation
  - FPGA-based or ASIC-prototype implementations of selected ULP modules and complete systems for case studies such as wearable health monitors and environmental sensors.
  - Quantitative evaluation of power consumption, energy savings, responsiveness, and reliability under real-world workloads.
- Academic and Industrial Impact
  - Contribution to the academic community through publications in peer-reviewed journals and conferences.
  - Potential for commercialization or integration into next-generation low-power edge computing platforms for wearables and smart IoT ecosystems.

8. Conclusion

This study underscores the importance of holistic low power design strategies for the successful deployment of sustainable, energy-efficient wearable and IoT solutions. As these technologies continue to evolve, research into intelligent and AI-assisted low power optimization techniques will play a pivotal role in shaping the future of smart, connected, and energy-conscious systems. This methodology ensures a multi-layered, holistic approach to ULP design, from transistor-level optimizations to system-level power intelligence, all tailored for resource-constrained, autonomous, and reliable operation in wearable and IoT environments. It will result in practical design solutions validated both through simulation and physical prototyping, ensuring both academic contribution and real-world relevance.

References

[1] B. Omkar L. Jagan, "Low-Power Design Techniques for VLSI in IoT Applications: Challenges and Solutions," J. Integr. VLSI, Embedded & Comput. Tech., vol. 1, no. 1, Apr 2024 ecejournals.in+1ijrmeet.org+1.

[2] "Efficient Integration of Ultra-low Power Techniques and Energy Harvesting in Self-Sufficient Devices," Sensors (MDPI), 2024 mdpi.com+1dr.ntu.edu.sg+1.

[3] X. Liu et al., "A Sub-μW Energy-Performance-Aware IoT SoC with a Triple-Mode PMU," IEEE J. Solid-State Circuits, 2024 rlpvlsi.ece.virginia.edu+1mdpi.com+1.

[4] "Low-power electronics," Wikipedia, 2024 onlinelibrary.wiley.com.

[5] "Deep-sub-voltage nanoelectronics," Wikipedia, 2023 link.springer.com+4en.wikipedia.org+4rlpvlsi.ece.virginia.edu+4.

[6] O. Faruqe et al., "A 10-Channel, 1.2 μW, Reconfigurable Capacitance-to-Digital Converter for Low-Power, Wearable Healthcare Applications," IEEE Biomed. Circ. & Syst. Conf., 2023 rlpvlsi.ece.virginia.edu.

[7] X. Wang and Q. Xu, "Multi-objective optimization in low-power VLSI design: Techniques and applications," IEEE Trans. CAD of Integr. Circuits & Syst., vol. 39, no. 11, 2020 ijrmeet.org.

[8] P. Shukla and A. Kumar, "Survey on power-efficient design techniques for IoT devices," Int. J. Low-Carbon Technol., vol. 15, no. 4, 2020 ijrmeet.org.

[9] M. Khan et al., "A Survey on RF Energy Harvesting System with High Efficiency RF-DC Converters," J. Semicond. Eng., 2020 arxiv.org+2mdpi.com+2link.springer.com+2.

[10] M. Caselli, M. Ronchi, A. Boni, "Power Management Circuits for Low-Power RF Energy Harvesters," J. Low Power Electron. Appl., 2020 mdpi.com.

[11] Low-Power VLSI Design for Next-Gen IoT Devices," IJRMEET, 2019 ijrmeet.org.

[12] M. Taghadosi et al., "High-Efficiency Energy Harvesters in 65 nm CMOS Process for Autonomous IoT Sensor Applications," IEEE Access, 2018 reddit.com+3mdpi.com+3link.springer.com+3.

[13] K. H. M. Rawy, "Ultra-low power energy harvesting and power management circuits for IoT applications," Ph.D. dissertation, Nanyang Technological University, 2018 dr.ntu.edu.sg.