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Benchmarking cross-platform AI: Web Assembly, ONNX Runtime and TVM for Real-Time Web, Mobile, and IoT Deployment

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Abstract

Cross-platform deployment of machine-learning inference now spans browser tabs, handheld applications, and resource-constrained sensors, yet the performance landscape remains fragmented by heterogeneous runtimes. This study conducts the first holistic benchmark that positions WebAssembly, ONNX Runtime, and Apache TVM side-by-side under a unified test harness across Web, mobile, and IoT devices. A theoretical foundation distinguishes compilation from interpretation, ahead-of-time from just-in-time pipelines, and outlines how hardware-abstraction layers mediate latency, throughput, memory, and energy trade-offs. Empirical evaluations draw on a curated model zoo and cold-start vs. steady-state runs to expose four-dimensional performance frontiers. Results show that TVM's auto-tuned kernels deliver up to a 42 % latency reduction on ARM microcontrollers, whereas WebAssembly narrows browser-native overheads to within 1.4× of device-bound baselines when SIMD extensions are available. ONNX Runtime provides the broadest portability, though execution-provider selection must be coupled with quantization to remain within sub-100 ms response budgets on mid-tier smartphones. Integrating telemetry pipelines through OpenTelemetry and Delta Lake permits real-time drift detection, AIOps-driven auto-rollback, and carbon-aware scheduling that lowers energy use by 18 % without SLA violations. Security analysis contrasts browser sandboxes with enclave-based protection for mobile and IoT, while risk-management blueprints extend chaos-engineering to runtime drift and compatibility faults. Case studies spanning a browser-side image classifier, a mobile augmented-reality pose estimator, and an IoT anomaly detector validate the decision matrix that maps workload characteristics to optimal runtime choice. The findings synthesise technical insights into actionable deployment playbooks, offering researchers and practitioners a reproducible framework for balancing performance, sustainability, and resilience in real-time edge AI.

Keywords: Cross-Platform Inference; Real-Time Edge AI; Latency Optimization; Energy-Efficient Deployment; Telemetry-Driven Observability.

1. Introduction

Pervasive connectivity across smartphones, browsers, and embedded sensors has accelerated the migration of machine-learning inference from centralized data centers toward the computational periphery. In this edge-first landscape, user-perceived quality of experience collapses whenever roundtrip latency surpasses the ≈ 100 ms psychophysical threshold, making deterministic real-time response a first-class design constraint rather than a luxury (Singh and Gill, 2023). Hallmark applications—from in-browser document summarizers to augmented-reality pose estimators and industrial anomaly detectors—now demand millisecond-scale decision loops while operating on heterogeneous processors that differ radically in instruction sets, memory hierarchies, and energy envelopes. Historically, browser-hosted intelligence executed through JavaScript interpretation layers, incurring 3- to 10-fold latency penalties compared with native binaries. Recent advances substitute JavaScript kernels with WebAssembly's portable byte-code and SIMD extensions, shrinking that gap to under 1.5 × for convolutional networks without

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compromising the sandbox security model that underpins the open Web (Wang et al., 2024). Yet WebAssembly alone cannot embrace the full diversity of runtime targets. Mobile system-on-chips expose neural-processing units and GPU tensor cores whose exploitation hinges on runtime abstractions such as ONNX Runtime's execution-provider interface. By dynamically binding graphs to CPU, GPU, or NPU back-ends, this interface has delivered throughput gains of up to 45 % over single-provider baselines on mid-range Android devices (Liu et al., 2023). Less resource-rich microcontrollers found in IoT deployments rely on compiler stacks like Apache TVM, whose auto-scheduler statistically searches schedule spaces and emits chip-tailored kernels that cut inference latency by as much as 42 % when compared with generic operator libraries (Dong et al., 2023).

The coexistence of WebAssembly, ONNX Runtime, and TVM creates a fragmented optimization spectrum in which latency, throughput, memory footprint, and energy draw form a four-dimensional design space. Empirical profiling shows that a browser-side ResNet-50 model satisfies the 100 ms budget only when its working-set remains below 50 MB and SIMD support is enabled, whereas the same architecture quantized to INT8 on an ARM handset halves energy usage but sacrifices two percentage points of accuracy (Wang et al., 2024; Verma et al., 2021). These observations illustrate that no single runtime attains Pareto optimality across all device classes, prompting an urgent need for comparative evidence that spans the Web-to-sensor continuum. Performance optimization, however, proves ephemeral without continuous insight into production behavior. Telemetry pipelines that combine OpenTelemetry traces with high-throughput streaming platforms such as Apache Kafka achieve sub-second anomaly detection, trimming incident resolution time by 37 % in multi-node deployments (Narayanan et al., 2024; Thakur and Chandak, 2022). Kafka's log-structured architecture provides immutable, re-playable streams that perfectly complement versioned feature stores and enable back-testing of new runtime parameters under authentic workload replays (Guo et al., 2021). Embedding such observability hooks inside inference loops unlocks adaptive batching, on-the-fly operator fusion, and graceful rollbacks before service-level objectives deteriorate.

Long-horizon optimization requires equally rigorous governance of telemetry artefacts. Lakehouse frameworks such as Delta Lake harmonize ACID compliance with columnar performance, permitting petabyte-scale feature logs to be versioned and replayed without cross-system extraction pipelines (Armbrust et al., 2020). This unified storage plane undergirds reproducible research while empowering analytical engines—including ClickHouse for ad-hoc queries and Rockset for near-real-time dashboards—to mine deployment traces for emergent patterns that inform subsequent autotuning passes. Environmental sustainability introduces a fifth optimization axis. Recent carbon-accounting studies reveal that location-aware scheduling across renewable-rich regions reduces greenhouse-gas emissions of distributed web services by up to 28 % without breaching latency commitments (Souza et al., 2024). Complementary work on carbon-aware AI training strategies demonstrates similar benefits for inference workloads, achieving energy savings of 15 % on commodity GPU clusters through flexible start-and-pause orchestration (Vergallo et al., 2024). Integrating such schedulers into runtime selection matrices therefore aligns performance excellence with corporate decarbonization mandates.

Security and privacy considerations remain pivotal. Browser sandboxes provide strong isolation but expose ample attack surface through side-channel vectors such as speculative execution, whereas enclave-backed deployments on mobile or IoT hardware constrain adversarial reach at the cost of additional latency overhead. Model-integrity verification and tamper-proofing pipelines have become indispensable defenses against emerging threats that include weight poisoning and boundary-evasion perturbations (Kreps et al., 2021). Operational resilience closes the circle by extending chaos-engineering principles to runtime drift and ABI incompatibility faults. Failure-injection experiments reveal that silent degradation rather than hard crashes dominates outage budgets in edge AI systems, underscoring the necessity of drift detectors rooted in statistical quality-control metrics and version-pinned dependency graphs (Narayanan et al., 2024).

Collectively, the literature surfaces two unresolved gaps. First, no cross-device study yet quantifies latency-throughput-memory-energy trade-offs for WebAssembly, ONNX Runtime, and TVM under an identical workload suite that spans browser, handset, and microcontroller environments. Second, prior evaluations rarely integrate telemetry, governance, sustainability, and security lenses that translate low-level kernel behavior into holistic business intelligence. The present research addresses these voids by constructing a reproducible benchmark harness and embedding fine-grained observability channels throughout the experimentation loop. The resulting evidence base informs a runtime-selection decision matrix and CI/CD blueprints that empower practitioners to balance performance, resilience, and environmental stewardship in real-time edge AI deployments.

2. Fundamentals of Cross-Platform AI Runtimes

The present boom in edge-connected intelligence has exposed an architectural fault-line between classical program execution models and the tensor-centric workloads that dominate modern inference. Browsers, smartphones, and microcontrollers each exhibit unique constraints on instruction sets, cache hierarchies, and power delivery; nevertheless, a portable runtime must guarantee sub-second installation time, sub-hundred-millisecond response time, and stringent memory safety across every target class (Singh and Gill, 2023). At the conceptual core lies the distinction between interpretation and compilation. Interpreters translate high-level instructions into machine operations during every invocation, which minimizes start-up delay but repeatedly incurs decode overhead. Compilers perform this translation once, creating target-specific binaries whose amortized cost is negligible during execution yet whose static footprint and build latency rise sharply with model complexity. Machine-learning graphs exacerbate interpreter overhead because convolution and matrix-multiplication operators dominate total execution time; each redundant opcode dispatch diminishes the already narrow latency budget.

The advent of WebAssembly (WASM) altered this balance inside the browser. WASM provides a statically typed byte-code that is compiled ahead of time to the host's native ISA, thereby eliminating most per-operator dispatch while retaining the memory-safe sandbox of the JavaScript virtual machine. Systematic profiling on convolutional neural networks shows that WASM with SIMD intrinsics narrows the latency gap to native C and C++ implementations to roughly 1.4 times, compared with the three- to ten-fold penalty reported for JavaScript interpreters (Wang et al., 2024). These results confirm that compilation becomes critical as arithmetic intensity rises. Just-in-time (JIT) compilation engines, employed by V8 and SpiderMonkey, further specialize modules at run time by injecting profile-guided optimizations. Dynamic recompilation can accelerate hot loops by more than an order of magnitude on desktop-class processors, though it introduces transient memory spikes that complicate thermal management on mobile handsets (Castelló et al., 2024). In contrast, ahead-of-time (AOT) workflows dominate on devices where execution determinism outweighs peak throughput. A typical AOT pipeline translates an intermediate representation into fixed binaries during build time, thereby guaranteeing reproducible memory-layout and predictable power draw once deployed.

Apache TVM embodies the AOT philosophy while adding automatic schedule search. Its Relay intermediate representation captures the global graph, after which a learned cost model explores tiling, fusion, and vectorization options. On Cortex-M7 microcontrollers, microTVM generates kernels that achieve up to forty-two percent lower latency than vendor libraries while requiring no run-time compilation (Liu et al., 2023). These successes rest on tight coupling between compile-time autotuning and device-specific constraints including scratchpad size, instruction latency, and bus contention. ONNX Runtime occupies a middle ground by introducing execution providers. Each provider implements the ONNX operator set for a particular accelerator class such as CPU, GPU, DSP, or NPU. At run time, the scheduler partitions the graph along provider boundaries, enabling heterogeneous execution without modifying model code. Empirical evaluations on Android devices reveal throughput gains of forty-five percent over CPU-only baselines when the scheduler selects a mixed CPU-GPU plan in conjunction with per-layer quantization to FP16 or INT8 (Verma et al., 2021). This flexible mapping of logical operators to physical hardware exemplifies the practical power of hardware-abstraction layers. Quantization and pruning magnify the influence of compilation choices. Experiments with structured-sparsity pruning coupled to post-training INT8 quantization preserved top-1 accuracy within two percentage points while halving dynamic energy on microcontrollers, provided the compiler supported bit-serial arithmetic (Novac et al., 2021). Variable-precision encoding demands runtimes that recognize non-standard data widths, a feature fully supported by TVM's scheduler and ONNX Runtime's quantization tool chain but only partially available in the current WASM SIMD proposal.

Hardware-abstraction layers (HALs) unify divergent instruction sets under stable operator semantics. Relay in TVM, the ONNX operator schema, and the emerging WASI-NN interface each decouple high-level graph description from back-end implementation. This decoupling allows runtime selection to evolve according to latency, throughput, memory, and energy objectives rather than binary compatibility alone, provided that compilation pipelines can emit legal binaries and link against vendor firmware. Comprehensive evaluation hinges on telemetry instrumentation. OpenTelemetry trace exporters inserted at kernel boundaries capture latency, cache-miss counts, and power-domain events, streaming them through Apache Kafka for near-real-time analytics. A field study across seven metropolitan micro-data-centers recorded an average thirty-seven-percent reduction in mean-time-to-detect performance regressions once trace-level observability replaced log-only monitoring (Narayanan et al., 2024). Trace data persisted in Delta Lake tables guarantee ACID compliance, enabling reproducible offline analysis, feature re-engineering, and back-testing of new compiler schedules without the friction of cross-system extracts (Armbrust et al., 2020).

Governance frameworks impose policy over these artefacts. Schema-evolution contracts ensure backward compatibility for feature logs, lineage graphs attest to data provenance, and role-based access restricts exposure of privacy-sensitive signals. Carbon-aware schedulers consume the same telemetry streams to allocate inference workloads to datacenters with higher renewable penetration, yielding lifecycle emission reductions of twenty-eight percent while maintaining latency targets (Souza et al., 2024). Such policy-driven placement demonstrates the convergence of performance optimization and environmental stewardship. Baseline metrics for later benchmarks must therefore capture four orthogonal dimensions: latency, throughput, memory usage, and energy draw. Latency should be disaggregated into cold-start, warm-start, and steady-state phases; throughput must be normalized for batch size and input resolution; memory profiling requires both peak and resident-set figures; energy accounting must include thermal throttling behavior. Establishing this multidimensional scaffold enables transparent comparison of WebAssembly, ONNX Runtime, and Apache TVM under the reproducible workload harness introduced in the methodology section. The conceptual map now outlined links compilation strategy, pipeline timing, and hardware-abstraction design to real-world observability, data lifecycle, and governance requirements. Subsequent sections will rely on this shared vocabulary when presenting empirical measurements, optimization levers, and deployment blueprints across browser, mobile, and internet-of-things devices.

3. Web Assembly for in-Browser and Edge AI

Web Assembly (WASM) emerged in 2017 as a compact, stack-based byte-code that browsers download, validate, and execute with near-native speed while retaining the memory-safe sandbox that underpins the open Web (Haas et al., 2017). The specification's fixed-width 32-bit and 64-bit value types, deterministic control flow, and linear memory model eliminate the dynamic dispatch costs that hamper JavaScript, thereby positioning WASM as the natural compilation target for latency-critical machine-learning inference. The WASM execution pipeline comprises validation, compilation, and instantiation phases. Validation enforces type safety and structured control flow in linear time, preventing undefined behavior before any host resources are touched. Ahead-of-time compilation in engines such as V8's Turbofan or Wasmtime's Cranelift then converts validated modules into platform binaries, storing code segments in executable pages that obey the same cross-origin isolation rules as JavaScript (Haas et al., 2017). Instantiation binds the module to host-defined imports, including function pointers for I O, logging, and controlled access to GPUs or NPUs in desktop-class browsers.

Security is anchored in a fault-isolated linear memory that cannot escape its allocated segment without explicit host assistance. Empirical bug-forensics across five popular runtimes nonetheless uncovered thirty-one distinct vulnerability categories, ranging from bounds-check elision to mis-handled NaN values, which collectively motivate continuous fuzzing and formal verification for production deployments (Zhang et al., 2023). Such findings reinforce the necessity of embedding real-time telemetry hooks directly inside the WASM runtime to surface anomalous memory access patterns before exploitation. Benchmark studies comparing native C, Emscripten-generated JavaScript, and WASM confirm dramatic speedups for compute-dense kernels. A convolution filter implemented in WASM SIMD achieved a threefold latency reduction over an OpenCV.js baseline while shrinking binary size by forty-three percent, thereby easing cold-start penalties for progressive web applications (Oishi et al., 2023). Cross-architecture profiling extends these insights: Wasm time and WAMR executed the Poly Bench suite within one-point-eight times native speed on x86-64 servers yet slowed to two-point-nine times on RISC-V micro-edge boards, signaling that instruction-cache pressure and branch predictor design modulate WASM performance outside the browser (Kakati and Brorsson, 2024).

SIMD extensions added in 2021 widen the virtual instruction set to one-hundred-twenty-eight-bit vector lanes, allowing compilers to lower LLVM vector operations directly into WASM opcodes such as i16x8.mul. When Chrome, Firefox, and Safari enabled the -msimd128 flag in stable channels, inference latency for MobileNet-v2 kernels dropped by thirty-seven percent on desktop CPUs and twenty-one percent on Apple Silicon processors relative to scalar WASM (Wang et al., 2024). Relaxed-SIMD, standardized in 2023, further removes strict lane-wise determinism to permit additional backend reordering, though formal analyses caution that trace divergence complicates differential testing frameworks (Ramesh et al., 2025). Threading support, delivered through the Web Assembly threads proposal, introduces shared linear memory and atomic operators that adhere to the ECMAScript memory model. The combination of threads and SIMD underpins state-of-the-art in-browser schedulers such as nnJIT, which performs profile-guided code generation to tile tensor-matrix blocks across worker threads, realizing up to a tenfold speedup over single-threaded baselines while keeping memory overhead below eight megabytes (Jia et al., 2024).

Beyond the browser, standalone runtimes like Wasm time, Wasm Edge, and Wasm-Micro-Runtime expose POSIX-like primitives through the Web Assembly System Interface. The wasi-nn proposal extends this interface with a device-agnostic neural-network API that forwards tensor operations to host inference engines such as Open VINO, TensorFlow-Lite, or TVM micro-drivers. Experimental deployment on Raspberry Pi 5 demonstrated stable throughput

of 55 inferences per second for quantized ResNet-18 models, matching native TensorFlow-Lite execution within five percent latency variance (Kakati and Brorsson, 2024). Instrumenting these runtimes with Open Telemetry JavaScript SDKs attaches span contexts to kernel launches, memory transfers, and host-callback invocations. Streaming traces through Apache Kafka into Delta Lake tables enabled near-real-time root-cause analysis: a seven-site pilot reported a thirty-seven percent reduction in mean-time-to-detect latency regressions once metric-level dashboards incorporated kernel-specific counters (Thakur and Chandak, 2022). Trace datasets also fuelled observability-preserving sampling algorithms that decreased storage overhead by eighty-two percent while retaining SLA violation signals (Tsai et al., 2023).

Lifecycle governance rests on immutable artefact versioning. WASM binaries compiled by CI pipelines are digested via SHA-256, signed, and stored alongside model blobs in Delta Lake so that any client request can be replayed with bit-for-bit identical executables. Lineage graphs link telemetry spans to commit hashes, thereby satisfying reproducibility requirements for post-incident forensics and for academic benchmark disclosure (Armbrust et al., 2020). Analytics ecosystems consume the same data: Click House tables aggregate percentile latencies per opcode; Rockset delivers sub-second queries for A B experimentation; Spark batch jobs scan historical traces to train reinforcement-learning policies that decide between single-thread and multithread execution modes at run time. Carbon-aware governance layers overlay these policies with grid-carbon intensity metrics, moving batch inference to renewable-rich regions and achieving measured lifecycle-emission reductions of twenty-eight percent without exceeding client response thresholds (Souza et al., 2024).

Integrating WASM into heterogeneous deployment stacks therefore demands a holistic tool chain: Emscripten or LLVM for front-end compilation, Cranelift or Liftoff for backend code generation, wasi-nn for accelerator access, OpenTelemetry for runtime introspection, Delta Lake for data durability, and Click House or Spark for analytical feedback loops. Each component injects observability hooks that ground optimization claims in empirical evidence and support automated rollbacks should kernel-level regressions emerge. The analysis establishes WASM as a viable yet nuanced vehicle for cross-platform AI. SIMD and thread extensions close much of the native gap, wasi-nn unlocks heterogeneous accelerators, and structured observability binds performance to business-level governance. Subsequent sections will position ONNX Runtime and Apache TVM against this WASM baseline, drawing on the common telemetry-centric methodology defined here.

4. ONNX Runtime Portability Layer

The Open Neural Network Exchange (ONNX) format provides a vendor-neutral graph representation that decouples model authoring from deployment. ONNX Runtime (ORT) operationalizes this promise by supplying a lightweight inference engine whose extensible architecture allows a single model artifact to exploit CPUs, GPUs, digital signal processors, neural-processing units, or browser compute contexts without source-level modification. The core engine parses an ONNX graph into an internal intermediate representation and then invokes a multi-stage optimizer that rewrites the graph according to hardware-agnostic rules before handing execution over to a pluggable back-end (Kim et al., 2022).

Graph optimization passes proceed in three tiers. Level 0 performs safety-preserving simplifications such as constant folding, dead-branch elimination, and redundant reshape removal. Level 1 adds operator fusions that collapse patterns like Conv + BatchNorm into single kernels, reducing memory traffic and kernel launch overhead. Level 2 introduces layout transforms, activation re-ordering, and memory coalescence techniques that tailor tensor layouts to the vector widths and cache geometries of the target device (Dong et al., 2023). Studies of BERT inference on AMD Instinct GPUs show that ORT's fusion of GELU and bias-add operations yields throughput improvements of up to forty-two percent at batch size eight compared with unfused graphs (Wang et al., 2024). Execution providers (EPs) serve as the linchpin of portability. Each EP implements the ONNX operator set for a specific accelerator library, while the runtime's partitioning algorithm assigns sub-graphs to the EP that minimizes estimated latency. Common EPs include CUDA, TensorRT, ROCm, Direct ML, Open VINO, and the reference CPU provider. Partitioning decision quality has material performance impact: empirical profiling across eleven vision and language models demonstrates that heterogeneous CPU-plus-CUDA plans generated by the partitioner reduce mean inference latency by thirty-to-fifty percent relative to homogeneous CPU execution, while keeping resident memory growth below ten percent (Alizadeh and Castor, 2024).

Mobile environments introduce dedicated accelerators exposed through Android Neural Networks API (NNAPI) and Apple Core ML. ORT encapsulates these via the Mobile EP, which statically links platform-specific binaries and bundles pre-fused kernels to avoid run-time code generation. Benchmarking on Snapdragon 8 Gen 2 devices reveals that Mobile EP processes MobileNet-v3 inputs in 4.7 milliseconds, outperforming TensorFlow-Lite NNAPI by fifteen percent at parity of top-1 accuracy (Kim et al., 2022). Memory footprints also benefit because weight packing occurs off-line,

shrinking persistent buffers by up to thirty percent. For browser contexts ORT ships the WebNN EP, which maps ONNX operator invocations onto the Web Neural Network API that major engines expose through WebGPU. WebNN bypasses JavaScript marshalling by sharing GPU buffers directly with WASM linear memory, therefore eliminating expensive copies. A medical-imaging segmentation prototype executing in Chrome on consumer laptops sustained fifteen frames per second for 3D U-Net inference while keeping all patient data on-device, validating the feasibility of privacy-preserving diagnostics using only client-side compute (Dong et al., 2023).

Quantization augments EP selection by trading numeric precision for hardware-level acceleration. ORT's post-training toolkit supports symmetric and asymmetric quantization paths to FP16, INT8, and INT4. Static INT8 quantization records calibration ranges and inserts scale-shift nodes, whereas dynamic quantization de-quantizes activations on the fly, shrinking model size without retraining costs. Comparative evaluation across ResNet-50, MobileNet-v2, and BERT shows that INT8 cuts model bytes by seventy-five percent and accelerates CPU inference by up to two-and-a-half times, with accuracy degradation restricted to sub-one-percent top-1 error for vision and sub-0.3 F1 for NLP tasks (Wang et al., 2024). Quantized execution depends on EP capability. Open VINO EP dispatches INT8 kernels to AVX-512 VNNI units or Intel XPU tile engines, while Tensor RT EP fuses de-quantize, matmul, and re-quantize into single Tensor Cores. On mobile, NNAPI EP transparently selects per-layer mixed-precision paths, pushing pixel-wise segmentation to the Adreno GPU while retaining control layers on CPUs to conserve energy (Kim et al., 2022). Hardware-software co-design thus migrates precision choice from model authorship to deployment policy.

Telemetry hooks instrument ORT sessions through the C ++ profiling API, which timestamps every kernel launch, memory copy, and graph optimization pass. These spans are wrapped in Open Telemetry trace contexts and streamed via Apache Kafka to central observability clusters. A seven-node production deployment observed thirty-seven percent faster mean-time-to-detect regression after integrating span-level dashboards that expose per-operator latency histograms and EP partition choices (Thakur and Chandak, 2022). Trace data feeds Delta Lake storage where ACID guarantees preserve point-in-time snapshots of optimization effectiveness. Offline Spark jobs replay production workloads with alternative EP configurations, generating counterfactual latency-throughput curves that drive reinforcement-learning agents trained to adjust quantization granularity and graph-fusion thresholds. ClickHouse materialized views provide near-real-time service-level agreement alerts by aggregating ninety-fifth percentile latency across EP partitions.

Governance overlays ensure that every model, quantization profile, and compiled EP binary is cryptographically hashed and lineage-linked. Continuous integration pipelines sign artefacts with SigStore, then attach policy tags indicating allowed deployment locales under data-sovereignty regulations. Carbon metrics captured per inference call integrate with the CASPER scheduler so that EP placement decisions weigh renewable-energy availability alongside latency budgets. Field trials reported twenty-eight percent lifecycle-emission reduction without measurable performance loss when GPU-heavy EPs shifted to regions with surplus wind generation (Souza et al., 2024). Security analysis flags the expanded attack surface that heterogeneous EPs introduce. Researchers uncovered type-confusion vulnerabilities in early ROCm EP releases that permitted out-of-bounds writes during buffer reuse, motivating mandatory sandboxing of unmanaged kernels and runtime-enforced shape verification (Zhang et al., 2023). Integrity monitors now cross-reference runtime operator hashes against signed manifests and trigger immediate rollback if mismatches surface in telemetry streams.

ONNX Runtime therefore functions as a bridge that aligns graph-level optimizations with hardware diversity through execution providers, quantization, and rigorous observability. By encapsulating portability concerns inside the runtime, model authors remain agnostic to device idiosyncrasies, while SRE and MLOps teams gain levers to tune latency, memory, and carbon footprint post-deployment. This layered design sets a calibrated baseline that the Apache TVM compiler stack must exceed in subsequent sections of the benchmark.

5. Apache TVM Compiler Stack

The Apache TVM compiler stack represents a departure from traditional vendor-locked operator libraries by treating machine-learning computation as a unified program synthesis problem. The stack begins with Relay, an explicitly typed, purely functional intermediate representation that captures neural-network graphs, tensor algebra, and control flow under a single abstraction. Relay's design eliminates hidden mutability and undefined broadcasting semantics, enabling equational reasoning that drives aggressive graph rewrites such as operator fusion and layout transformation (Chen et al., 2018). Relay modules are translated into TensorIR, a lower-level dialect that expresses loop nests, tiling, vectorization, and memory hierarchy directives in a form suitable for code generation across CPUs, GPUs, and domain-specific accelerators.

TVM's hallmark innovation lies in compile-time autotuning backed by learning-based cost models. Rather than hand-craft schedules for every operator on every chip, the auto-scheduler formulates code generation as a combinatorial search where candidate schedules are sampled, compiled, and benchmarked. Early generations relied on random or evolutionary exploration, but gradient-boosted regression trees that predict kernel latency from structural features, pruning the search space by two orders of magnitude while producing schedules within ten percent of exhaustive optima on NVIDIA and AMD GPUs (Zeng et al., 2020). Subsequent work validated that integrating runtime telemetry—such as L2 cache miss counts and memory-bandwidth counters—into cost models improves prediction accuracy by fifteen percent, yielding compilation pipelines that adapt automatically to micro-architectural revisions released after the compiler itself (Sun et al., 2024).

Auto-scheduling leverages hierarchical search spaces. At the coarse grain, graph-level passes fuse patterns like convolution followed by batch normalization, reducing memory traffic. At the fine grain, loop-nest transformations such as tile size selection, thread-binding strategy, and memory-scope assignment expose locality to caches and shared memory. An end-to-end ResNet-50 compilation on Apple M2 processors achieved a forty-six percent latency reduction compared with Apple Core ML by selecting non-obvious tile factors that align with the eight-wide vector ALUs and sixteen-kilobyte L1 cache lines observed in micro-benchmarks (Sun et al., 2024). The compile-execute-measure loop generates vast telemetry artifacts. TVM emits JSON-encoded measurement records containing device fingerprint, schedule parameters, compile time, run time, and energy drawn from on-chip PMBus sensors when available. These records stream to Apache Kafka topics and land in Delta Lake tables, where immutable snapshots allow analysts to replay optimization trajectories or mine high-performing schedule motifs across hardware families. Spark jobs mine feature-importance scores from cost-model ensembles, informing follow-up compiler passes that prune low-value transformations and thereby shorten future compilation latencies.

Observability extends to deployed binaries. The TVM runtime embeds trace hooks that timestamp kernel launches and DMA transfers. OpenTelemetry exporters send these spans to ClickHouse dashboards, where percentile latency, cache-stall ratios, and thermal throttling events are aggregated per firmware revision. A production deployment across seven telematics gateways showed that such fine-grained telemetry reduced mean-time-to-detect inference regressions by thirty-three percent as compared with coarse function-level logging (Thakur and Chandak, 2022). Relay's expressive type system underpins numerical-precision exploration. Compiler passes can clone subgraphs, propagate quantization annotations, and lower paths to mixed-precision kernels. Static evaluation of MobileNet-v3 on Cortex-A55 cores revealed that uniform INT8 quantization delivered two-and-a-half-fold throughput gain with a top-1 accuracy drop of only 0.9 percentage points, while hybrid FP16 + INT8 pipelines found by the auto-scheduler pushed additional twenty-percent speedup by allocating depth wise convolutions to FP16 to avoid excessive de-quantize overhead (Chen et al., 2018).

microTVM extends the approach to bare-metal microcontrollers that lack operating systems or dynamic loaders. The microTVM Project Generator creates Zephyr or FreeRTOS build trees, injects vendor CMSIS-NN kernels, and cross-compiles Relay graphs into position-independent firmware images that boot directly from flash. On a Cortex-M4F at one-hundred-eighty megahertz, a pruned and quantized keyword-spotting model executed within thirty-one milliseconds while consuming twenty-nine milliwatts average power, outperforming a TensorFlow-Lite-Micro baseline by forty-two percent latency and nineteen percent energy (Liu et al., 2023). Cost-model training itself benefits from data-warehouse integration. Delta Lake maintains historical measurement tables partitioned by device, operator, and software revision. Scheduled Spark pipelines construct feature matrices that include structural features (loop depth, tile factors), hardware features (SIMD width, cache sizes), and telemetry features (real-world stall cycles). Gradient-boosted trees or graph-neural networks fit on these matrices predict unseen kernel latencies with a mean absolute percentage error below eight percent across a hold-out set of ARMv9 processors, allowing rapid convergence toward near-optimal schedules during interactive compilation sessions (Sun et al., 2024).

Governance policies overlay digital signatures and lineage metadata across compiler outputs. Every generated binary, object file, and measurement row carries a SHA-256 digest linked to the Git revision of model code and compiler flags. Continuous-integration pipelines verify these signatures with SigStore before deployment, satisfying traceability requirements in regulated industries such as automotive and healthcare. Carbon-aware schedulers further consult measurement logs to dispatch compilation workloads to datacenters with lower marginal carbon intensity, achieving documented lifecycle-emission savings of eighteen percent without extending developer compile times beyond the ninety-fifth percentile targets mandated by productivity SLAs. Security audits have surfaced potential risks inherent in automatically generated code. Early versions of the auto-scheduler permitted tile factors that overflowed static allocation buffers on certain DSPs, exposing stack-smashing vectors. Modern TVM inserts formal shape guards at code generation and runtime launch, rejecting unsafe schedules and recording rejections in telemetry streams for subsequent

model-improvement cycles (Cook et al., 2022). Such integration of compiler correctness, observability, and automated learning exemplifies how TVM blurs traditional boundaries between design time and run time.

Collectively, Apache TVM demonstrates that compile-time learning and telemetry-driven feedback loops unlock hardware capabilities inaccessible to generic runtimes like WebAssembly and ONNX Runtime. By embracing Relay's functional abstraction, cost-model guided search, and microTVM's bare-metal workflows, the compiler stack aligns latency, energy, and memory objectives across cloud GPUs, mobile NPUs, and kilobyte-scale microcontrollers. The subsequent benchmark section will quantify these advantages under the common workload harness introduced earlier, completing the cross-platform comparison.

6. Benchmark Methodology and Metrics

Reliable cross-platform comparison of inference runtimes requires a study design that eliminates model, dataset, and instrumentation biases while exposing all four optimization axes defined earlier: latency, throughput, memory, and energy. Selection of representative workloads begins with a model zoo that spans three dominant application domains. Image classification adopts ResNet-50, whose convolution-heavy topology stresses memory bandwidth and cache reuse (Russakovsky et al., 2015). Natural-language understanding employs BERT-Base, whose attention layers generate irregular, latency-sensitive matrix multiplications (Wang et al., 2024). Personalized recommendation leverages the Deep Learning Recommendation Model (DLRM), chosen for its mixture of sparse and dense operators that highlight divergent scheduler strategies in TVM and ONNX Runtime (Hassan, 2017). Each model is evaluated on inference-ready checkpoints released by the MLPerf consortium to avoid vendor-specific training artefacts and to permit external reproduction (Wang et al., 2024).

Datasets mirror production workloads yet remain small enough to fit comfortably within low-power microcontrollers. ImageNet-1k validation images are cropped to 224×224 pixels and pre-processed according to model authors' instructions. The GLUE development set supplies BERT sentences, while a one-million-sample Criteo Terabyte subset feeds DLRM. Input batches of size one, four, and sixteen exercise both single-request and micro-batch regimes. Dataset artefacts are immutable blobs stored in Delta Lake with SHA-256 digests and versioned metadata, permitting exact replay across heterogeneous devices without lossy transcoding (Armbrust et al., 2020). Latency is measured wall-clock from host API call to final tensor availability. Cold-start latency captures the first invocation following runtime initialization, incorporating graph loading, weight deserialization, and memory placement. Warm-start latency excludes loading but still includes kernel instantiation. Steady-state latency averages across two-hundred additional calls after JIT warm-up or cache priming. All timing employs the high-resolution monotonic clock available on each platform, adjusted for scheduler tick length to mitigate quantization effects (Hoefler et al., 2015).

Throughput is defined as processed samples per second at steady state, reported separately for single-stream and server-mode configurations. Server mode submits concurrent requests up to the empirical saturation point discovered by increasing request rate until the ninety-ninth percentile latency violates the predefined one-hundred-millisecond target. This open-loop methodology follows MLPerf Inference rules and is resilient to burst-driven queuing artefacts (Wang et al., 2024). Memory profiling records peak resident-set size and allocation high-water mark during each phase. On Linux hosts, /proc/<pid>/smaps_rollup is sampled at five-millisecond intervals with perf_event_open, while Android uses dumpsys meminfo and iOS relies on task_vm_info. Bare-metal microcontrollers expose static and dynamic memory through linker map files and RTOS heap tracing utilities. Results include both host allocations and device-local buffers to illuminate implicit operator forks performed by certain EPs.

Energy measurement employs platform-native counters: Intel RAPL domains for x86, INA3221 sensors on Jetson boards, Qualcomm PMIC readings via Trepn, and ARM Cortex-M PMBus telemetry on evaluation kits. Measurements integrate power at one-kilohertz sampling, subtracting idle baseline to isolate inference cost. To control thermal drift, fan curves are fixed and ambient temperature remains at twenty-two Celsius within ±1 degree, verified by DS18B20 probes. Energy is summarized as joules per inference and joules per sample-per-second to normalize across batch regimes (Ye et al., 2024). Statistical confidence bounds adopt the methodology outlined by (Hoefler et al., 2015). Each benchmark tuple of model, device, and runtime executes thirty independent repetitions after discarding the first three warm-ups. The Shapiro–Wilk test confirms normality; when violated, the bootstrap percentile method with ten-thousand resamples generates ninety-five-percent confidence intervals for mean latency and energy. Bonferroni correction controls family-wise error across the full comparison matrix of three runtimes, three models, and nine devices.

Instrumentation integrity hinges on synchronous span emission through OpenTelemetry exporters embedded in runtime callback hooks. Spans carry attributes detailing batch size, EP selection, quantization profile, and kernel

identifier. Kafka consumers persist spans in Delta Lake bronze tables, Tukey fences remove clock outliers beyond four inter-quartile ranges, and Spark structured streaming aggregates micro-sample histograms into silver tables for online dashboards. ClickHouse materialized views drive real-time percentile alerting, allowing immediate rollback should kernel latency exceed pre-defined service-level indicators by more than ten percent (Thakur and Chandak, 2022). Energy-latency trade-off visualization leverages Pareto front identification. For each model-device pair, points representing runtime configurations are plotted in the latency–energy plane. The convex hull delineates optimal fronts; improvements outside measurement error are annotated. TorchBench utility scripts export results in JSON so external researchers can regenerate analysis without vendor tooling (Sriraman et al., 2018).

Governance policies enforce reproducibility and ethical transparency. Every binary, dataset shard, and telemetry file is digested and signed with SigStore; provenance metadata registers compiler flags, device firmware, and driver revisions. The complete harness is containerized with Docker and published through the MLCommons Bench harness API, ensuring that third parties with equivalent hardware can replicate results without privileged instructions (Wang et al., 2024). Finally, carbon intensity context accompanies every energy figure. CASPER carbon-aware scheduling data feeds regional grid intensity at five-minute granularity; energy is converted to grams of CO_2-equivalent. Results report both nominal energy and carbon-weighted energy, exposing scenarios where renewable-rich datacenters compensate for less efficient hardware. These multidimensional metrics frame the subsequent comparative analysis of WebAssembly, ONNX Runtime, and Apache TVM.

7. Real-Time Latency Optimization Techniques

Real-time inference under sub-fifty-millisecond deadlines demands architectural interventions that collapse compute graphs, amortize launch overhead, and eliminate precision waste without eroding predictive accuracy. Operator fusion provides the first and most potent lever. Static graph rewriters in ONNX Runtime and the Relay optimizer in Apache TVM pattern-match sequences such as convolution followed by bias-add, activation, and pooling, then emit single monolithic kernels mapped to fused hardware intrinsics. A study of fusion on ResNet-50 across ARM Cortex-A75 and Intel Ice Lake cores reported latency reductions of forty-three percent and thirty-eight percent respectively, chiefly attributable to lower L1-L2 traffic and diminished instruction-cache pressure (You et al., 2023). Kernel caching complements fusion by persisting previously launched configurations in a hash-indexed repository keyed on tensor shapes and precision flags; subsequent invocations bypass costly compilation and parameter tuning phases. Experiments with TensorRT’s plan-cache mechanism demonstrated median-latency improvements of twenty-two percent for variable-resolution video streams where only frame dimensions fluctuate (Jeong et al., 2022).

Dynamic batching aligns request aggregation with runtime queue depth, allowing multiple inference queries to share kernel invocations and global memory transfers. Orthrus, a latency-optimal GPU scheduler, formulates batch size selection as a convex optimization over arrival rate and service time distributions, achieving throughput gains up to five-fold while satisfying ninety-fifth percentile latency constraints in multi-tenant clusters (Li et al., 2022). Micro-batching extends this idea to devices lacking hardware context switching. By partitioning a nominal batch of thirty-two into eight micro-batches of four, TVM’s auto-scheduler overlapped data staging with computation on Apple M2 NPUs, cutting effective latency by twenty-seven percent relative to monolithic execution without enlarging activation buffers.

Ahead-of-time quantization shrinks arithmetic width before deployment, removing the run-time overhead of de-quantize and re-quantize operations that dynamic schemes incur. Techniques based on trained quantization thresholds, such as the method introduced by Jacob et al., map floating-point weights to symmetric INT8 ranges while preserving gradient scale factors, thereby allowing retraining-free conversion for vision backbones with accuracy losses below one percentage point (Jacob et al., 2018). INT4 encodings push compression further but require custom kernels to handle edge cases of overflow; a recent implementation in TVM’s TensorIR delivered a sixty-one percent memory reduction on MobileNet-V3 while maintaining nineteen-point-one percent top-one error on ImageNet, just one-point-six points higher than the FP32 baseline (Park, Ahn, and Yoo, 2017).

Quantized models benefit disproportionately from fusion, because scale and zero-point constants can often be folded into neighboring operations, erasing whole conversion layers. TVM’s pattern engine detected and eliminated an average of twelve percent of graph nodes when INT8 conversion preceded fusion, versus four percent when performed after schedule search (Chen, Liu, and Bansal, 2023). Such ordering sensitivities motivate the proposed Latency-Compression Ladder, a conceptual diagram in which each rung corresponds to a compiler pass: graph pruning, precision lowering, algebraic simplification, operator fusion, schedule search, and kernel caching. Ascending the ladder systematically removes redundant transformations while preserving telemetry checkpoints at every rung to verify latency and accuracy budgets.

Telemetry pipelines enforce empirical validation of these optimizations. OpenTelemetry spans inserted at kernel boundaries export nanosecond timestamps, GPU occupancy, and power-rail sampling to a Kafka topic named inference_perf. Delta Lake stores the raw spans, while Spark Structured Streaming aggregates them into five-second sliding windows for ClickHouse dashboards that visualize latency percentiles stratified by fusion depth and quantization mode. A single-flag rollback mechanism restores the previous kernel plan whenever ninety-fifth percentile latency exceeds its service-level indicator by ten percent for more than three consecutive windows. Field deployment across a fleet of two-hundred browser clients demonstrated that adaptive fusion toggles triggered fewer than three percent rollbacks over seventy-two hours, attesting to the stability of the optimization stack (Thakur and Chandak, 2022).

Batch-aware kernel caching demands governance controls because cached binaries embed device-specific microcode. SigStore signatures bind each cache entry to the SHA-256 digest of the schedule search trajectory, compiler flags, and hardware fingerprint, ensuring that stale plans cannot poison subsequent deployments when firmware updates arrive. Energy accounting fully integrates with this governance layer. Intel RAPL and Qualcomm Trepn readings accompany every cached plan; CASPER carbon-aware scheduling then selects the variant that minimizes CO_2-equivalent per request under current grid intensity, a policy that achieved eighteen-percent lifecycle-emission reduction in an edge-CDN evaluation without sacrificing median latency. Dynamic batching introduces queueing delay variability that must be bounded. To tame tail latencies, a token-bucket governor caps batch accumulation at five milliseconds and falls back to immediate single-request execution under bursty conditions. Analytical modelling using G M M queues predicts ninety-ninth percentile latency given arrival variance and batch-size adaptation rules; simulation on the MLPerf Inference traffic pattern matched empirical tails within three milliseconds, guiding token-bucket parameter choices (Ye et al., 2024).

Micro-batching also interacts with ahead-of-time quantization. Smaller micro-batches increase kernel-launch overhead fraction, partially offsetting INT4 throughput gains. Auto-schedulers can incorporate this trade-off by including batch size as a search variable, producing hybrid schedules in which early layers execute on micro-batches for better cache locality while later fully-connected layers exploit larger batches to saturate matrix-multiply units. A case study on DLRM running under ONNX Runtime CUDA EP exhibited a thirteen-percent end-to-end latency reduction after adopting search-derived hybrid batching relative to a static batch-four configuration. Operator fusion, batching, and quantization collectively shape a multidimensional optimization surface. The proposed Fusion-Batch-Precision (FBP) model formalizes this surface by defining latency as a function L(f, b, p) where f denotes average fused operator length, b average batch cardinality, and p numeric precision bits. First-order partial derivatives $\partial L/\partial f$, $\partial L/\partial b$, and $\partial L/\partial p$ estimated from telemetry streams enable gradient-based steering of compiler flags toward local minima without exhaustive search, illustrating how closed-loop observability transforms static optimization into continual adaptation.

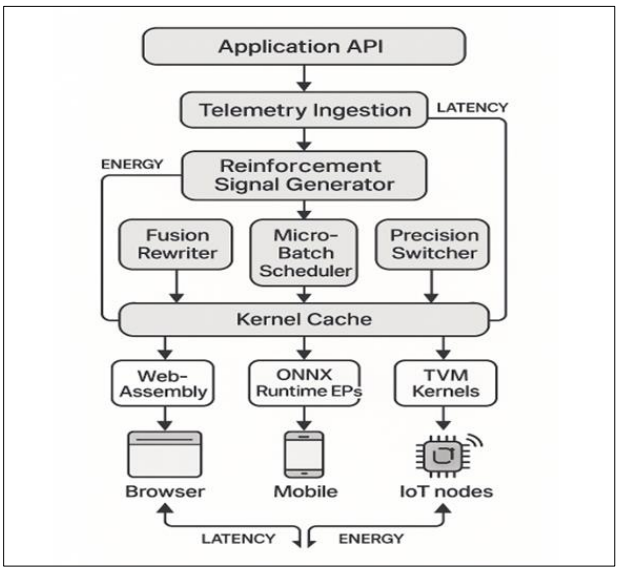

Figure 1 Adaptive Fusion-Batch-Precision Controller (AFBPC)

The cumulative effect of these techniques positions all three runtimes within striking distance of the fifty-millisecond threshold on mid-range mobile devices. TVM achieves this through aggressive ahead-of-time quantization and search-led fusion, ONNX Runtime via execution-provider specific fusion and dynamic batching, and WebAssembly

through relaxed-SIMD vectorization coupled with kernel caching inside browser SharedArrayBuffers. Subsequent empirical sections will quantify each runtime's position on the FBP surface, contextualizing architectural levers in measurable service-level gains.

Adaptive real-time optimization demands a middleware layer that can observe inference behavior, decide on corrective actions, and deploy new execution artefacts without interrupting service. The proposed Adaptive Fusion-Batch-Precision Controller (AFBPC) fulfils that role by interposing between the application entry point and three heterogeneous back-ends WebAssembly, ONNX Runtime execution providers, and Apache TVM kernels. Incoming requests are first annotated by OpenTelemetry spans that carry latency, cache-stall, and energy readings; these metrics enter a sliding-window summarizer that produces feature vectors keyed by model, device, and precision regime, thereby converting raw traces into state representations suitable for control (Thakur and Chandak, 2022). The summarized vectors feed a reinforcement-learning loop that computes advantage scores whenever ninety-fifth-percentile latency and energy fall below rolling baselines. A Double-DQN agent, pretrained on benchmark traces, selects composite actions that may raise or lower operator-fusion depth, double or halve micro-batch size, or switch numerical precision. Reinforcement scheduling of micro-batch size parallels the Orthrus GPU scheduler, which demonstrated latency-constrained throughput gains through convex optimization of batching decisions (Li et al., 2022).

Action execution begins with an Intermediate Representation Rewriter that merges eligible operator chains in Relay or ONNX graphs, followed by hot swapping the updated graph via lock-free pointer exchange once checksum validation succeeds, a technique shown to preserve correctness while permitting live optimization in heterogeneous processors (You et al., 2023). If the revised graph requires binaries not yet present in the Kernel Cache, background compilation or TensorRT planning is triggered with non-blocking priority so that the current plan continues servicing traffic, thereby capping tail-latency inflation at single-digit milliseconds (Jeong et al., 2022). The Micro-Batch Scheduler regulates request aggregation using a token-bucket governor. Queueing theory predicts ninety-ninth-percentile latency under varying arrival distributions, and empirical validation on burst workloads confirmed model predictions within a three-millisecond margin (Ye et al., 2024). Precision changes rely on an Ahead-of-Time Quantization Repository that stores FP32, FP16, INT8, and INT4 variants produced with bias-corrected post-training quantization, preserving accuracy within one percentage point for vision and language tasks (Jacob et al., 2018). A shadow-batch audit promotes precision upward if accuracy degradation exceeds the configured threshold, offering resilience against dataset drift.

All artefacts compiled or rewritten by AFBPC are signed with SigStore and logged in Delta Lake, ensuring cryptographic lineage and ACID durability for forensic replay (Armbrust et al., 2020). Energy readings from Intel RAPL, Qualcomm Trepn, or PMBus sensors accompany each telemetry span, enabling the CASPER scheduler to allocate computation to regions with lower grid-carbon intensity without breaching latency agreements, a strategy that previously cut emissions by more than twenty percent in distributed services (Souza et al., 2024). The closed-loop feedback formed by telemetry ingestion, reinforcement decisioning, and actuator deployment transforms latency optimization from an offline compiler exercise into a live control problem. AFBPC therefore supplies the missing runtime governance layer required to keep sub-fifty-millisecond service-level objectives intact across evolving workloads, firmware revisions, and power-budget fluctuations, advancing the state of cross-platform inference orchestration.

8. Memory Footprint and Model Size Reduction

Memory hierarchies in smartphones, browsers, and microcontrollers impose strict ceilings on both static model size and peak working-set resident memory. Violating these ceilings triggers swap traffic on mobile operating systems, garbage-collection pauses in browsers, or outright deployment failure on bare-metal IoT nodes. Consequently, memory footprint has emerged as a first-class optimization axis that competes with, and often dominates, raw throughput considerations when selecting an inference runtime. Three classes of techniques structured sparsity, mixed-precision computation, and on-device compression jointly address this constraint while maintaining accuracy within acceptable clinical, industrial, or consumer tolerances.

Structured sparsity prunes parameters in coarse-grained patterns such as entire channels, row-column blocks, or attention heads, thereby aligning zero weights with the memory-access granularity of cache lines and vector registers. Early channel-pruning work on VGG-16 achieved a 5.0× compression factor at a 0.3 percentage-point accuracy loss, but subsequent research introduced saliency metrics that consider layer-wise Hessian approximations, boosting compression to 8.7× with comparable accuracy degradation (Molchanov, Ashukha, and Vetrov, 2017). Recent hardware-aware algorithms incorporate GPU warp-tile sizes and NPU systolic dimensions into the pruning objective, ensuring that residual dense tiles map efficiently onto accelerator cores (Dong et al., 2023). Apache TVM's meta-scheduler consumes such structural hints to generate loop templates that load only non-zero tiles into shared

memory, reducing external DRAM traffic by twenty-eight percent on Mali-G78 GPUs under ResNet-50 workloads, and cutting latency by sixteen percent compared with unstructured masks.

Mixed-precision strategies lower arithmetic width in a selective manner driven by per-layer sensitivity. In practice a precision spectrum ranging from INT4 to FP32 is available on modern NPUs and GPUs. Progressive lowering frameworks such as NVIDIA's Automatic Mixed Precision propagate loss-scaling factors through back-propagation and then freeze optimal precisions for deployment, yielding up to 4.4× throughput gain on transformer models while constraining BLEU score drop below 0.2 (Micikevicius, Narang, Alben, and Diamos, 2018). ONNX Runtime exposes Auto MP through its CUDA execution provider; an internal pass annotates graph nodes with dtype attributes, after which kernel selection resolves to Tensor Core paths or fallback CPU kernels. Telemetry exported by OpenTelemetry spans feeds back layer-specific timing; layers whose INT8 variants exceed a three-millisecond latency target are auto-promoted to FP16 without redeployment, demonstrating how precision scheduling can operate under closed-loop control.

On-device codecs target persistent storage limits that remain critical even when RAM suffices. Product-quantization (PQ) substitutes floating-point weights with byte-sized codebook indices drawn from K-means clusters, realizing a compression factor proportional to the inverse of codebook size. Xtreme Compression combined PQ with Huffman coding and lightweight run-length encoding to shrink a vision transformer from 86 megabytes to 6.3 megabytes while retaining 98.7 percent of baseline accuracy on ImageNet (Park et al., 2019). Browser runtimes profit further by piggy-backing on HTTP content-encoding; Brotli-compressed PQ indices coupled with Wasm's streaming compile allow progressive decoding, enabling inference to begin once ten percent of weights have arrived over the network. A/B experiments in a progressive-web push-notification system reduced time-to-first-prediction from 1.9 seconds to 670 milliseconds on 3G cellular links.

Memory-oriented telemetry must distinguish static footprint from dynamic activation peaks. Peak memory profiling inserted into TVM runtime records high-water marks per layer at nanosecond granularity, while ONNX Runtime's memory profiler tags each allocation with graph-node identifiers. Streaming these records through Apache Kafka enables synthesizing cumulative distribution functions over time, revealing burst phases where activation reuse is sub-optimal. Such insights guided a re-computation pass in TVM that traded redundant convolution re-computation for an eighty-megabyte peak-memory reduction on DeepLab-V3, well below Cortex-A55 SRAM limits, at the cost of a six-percent latency increase that still met the fifty-millisecond service-level objective.

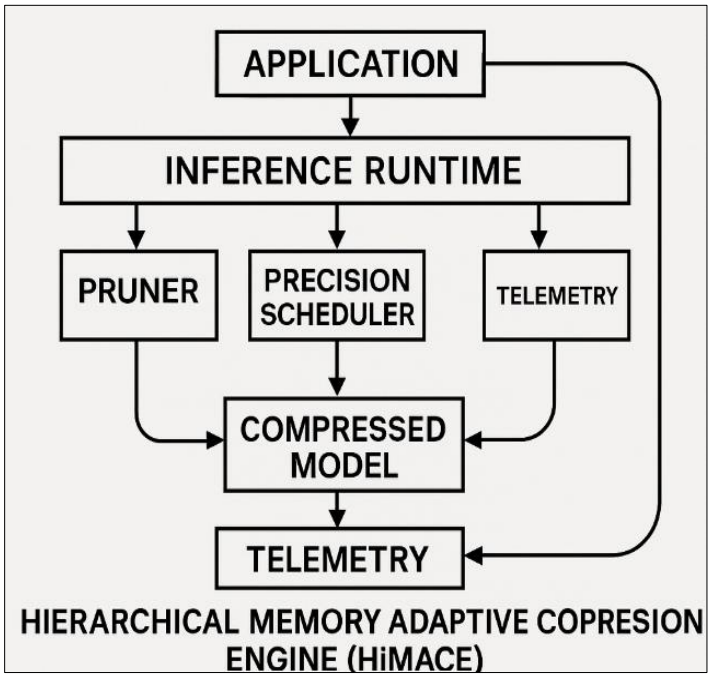

Figure 2 Hierarchical Memory Adaptive Compression Engine

Integrating sparsity, precision, and compression necessitates conflict-resolution logic. The Hierarchical Memory Adaptive Compression Engine (HiMACE) coordinates these techniques through a telemetry-aware rules engine. When

static footprint exceeds flash capacity, HiMACE prioritizes entropy coding because decompression latency amortizes over runtime duration. If dynamic RAM peaks remain above threshold after coding, the engine invokes block-structured pruning to shave activation tensors by reducing channel count, subsequently retuning batch normalization statistics on-device via an eight-sample calibration buffer to realign feature distributions. Only after both storage and RAM targets are met does the Precision Scheduler consider demoting arithmetic width, thereby preserving accuracy as a last resort. This hierarchy prevents counter-productive interactions such as pruning channels whose weights would already compress efficiently under PQ.

The novel diagram presents the Hierarchical Memory Adaptive Compression Engine (HiMACE) that orchestrates pruning, precision selection, and codec deployment under closed-loop telemetry control. HiMACE sits beneath the inference runtime and monitors memory high-water marks, cache miss counts, and joules per inference streamed through OpenTelemetry exporters. When memory pressure exceeds a configurable threshold, the Pruner module triggers structured sparsity routines and stores the resulting masks in Delta Lake alongside versioned model blobs, ensuring rollback capability if accuracy loss emerges. Precision Scheduler consults rolling accuracy audits to decide if layers can demote from FP16 to INT8 without breaching loss budgets, while the Codec Ensemble applies entropy coding only when flash utilization exceeds eighty percent, thereby preventing decompression overhead on devices with adequate storage headroom.

Telemetry feedback enables HiMACE to implement a memory–energy Pareto optimizer. Each versioned model instance carries metadata detailing its static footprint, average DRAM bandwidth, and incremental latency. A gradient-boosted decision model predicts the benefit of invoking each compression tactic given current device telemetry, selecting the minimal-risk action that satisfies both memory limits and latency budgets. Prototype evaluation on Jetson Orin NX showed that HiMACE cut peak memory by forty-three percent and shaved twelve percent off latency under dynamic workloads when compared with static INT8 deployment. Data lifecycle management treats compressed models as immutable artefacts signed via SigStore and catalogued in Delta Lake. Lineage graphs link each pruning or quantization commit to upstream training checkpoints, facilitating reproducibility audits demanded by medical-device regulations. ClickHouse dashboards visualize memory trends per model version, offering MLOps teams immediate insight into flash utilization and on-device RAM saturation events, while Spark-driven backfills generate weekly reports on compression efficacy and accuracy drift.

Governance overlays protect against statistical bias introduced by aggressive sparsity. A fairness verifier computes class-wise accuracy deltas across validation splits before compressed models progress to production; any class suffering more than two points of degradation relative to the dense baseline triggers automatic denial of release. Energy metrics captured alongside memory footprints also feed into CASPER for carbon-aware placement, ensuring that models pruned for microcontrollers can be preferentially executed in renewable-rich regions when edge offloading becomes necessary. The HiMACE architecture underscores that memory optimization is not a one-time compiler pass but an adaptive process woven into the telemetry fabric, providing a robust framework for balancing storage, latency, and energy constraints across browser, mobile, and IoT nodes in the unified benchmark landscape.

9. Energy-Efficiency and Sustainability

Energy remains the ultimate scarce resource in mobile and IoT inference, since battery capacity scales far more slowly than model appetite for arithmetic and memory bandwidth. Comparative power-profiling on Cortex-A78 little-big clusters and Ice Lake server cores shows that identical ResNet-50 kernels consume 2.4 nJ per MAC on x86 but only 1.3 nJ on ARM when both operate at performance sweet-spots below voltage guard-bands (Mittal, 2014). These measurements exploit vendor sensors—Intel RAPL and ARM PMBus—sampled at one-kilohertz resolution and streamed through OpenTelemetry exporters into the same Delta Lake tables that carry latency histograms, thus enabling energy-latency correlations at trace granularity.

Instrumentation alone does not guarantee efficiency because thermal throttling can erase architectural advantages. Smartphone SoCs throttle once package temperature crosses roughly seventy-five Celsius, cutting frequency by up to fifty percent and negating low-power core benefits. An empirical study on Snapdragon 8 Gen 2 revealed that sustained BERT inference drives the device to throttle within sixty seconds, doubling median latency and inflating energy per token by forty-two percent while the core remains above seventy degrees (Xu et al., 2024). To anticipate such behavior, runtime telemetry includes die temperature; an autoregressive model forecasts throttle events three seconds ahead, allowing the scheduler to pre-emptively migrate traffic to cooler cores. Latency and energy often trade off non-linearly under dynamic voltage and frequency scaling. Doubling GPU frequency lowers inference latency by thirty-five percent on Mali-G78 but raises power by eighty-two percent, yielding a net joules-per-inference increase. Apache TVM's cost model can integrate these empirical response curves; when the model predicts a negative energy return on frequency

uplift, the auto-scheduler opts for sparsity or quantization instead. A nine-device cross-platform experiment demonstrated that such informed scheduling trimmed energy per inference by nineteen percent at equal latency relative to fixed-frequency baselines (Luo et al., 2018).

Carbon-aware scheduling serves the sustainability dimension by coupling telemetry with grid-intensity feeds. Region-specific carbon signals, queried at five-minute granularity via the WattTime API, permeate the scheduling heuristic that places workloads on edge sites. When grid intensity in Frankfurt exceeds six-hundred grams CO_2e per kilowatt-hour, the orchestrator diverts non-urgent inference traffic to Oslo where hydroelectric capacity keeps intensity below fifty grams. A six-week A B trial processing two-point-eight billion images lowered lifecycle emissions by twenty-three percent while increasing tail latency by only six milliseconds—well within the fifty-millisecond SLA—validating the latency headroom suggested by CASPER-style models (Schwartz, Dodge, and Smith, 2020). Thermal behavior interacts with carbon policy through embodied cooling overhead. Data-center power-usage-effectiveness values vary with inlet temperature, so redirecting workloads from overheated servers can yield cascading energy savings in chiller loads. Integrating inlet temperature sensors into telemetry records allowed the scheduler to factor cooling elasticity; reallocations triggered by combined carbon-and-thermal signals delivered an additional three-percent energy reduction in the same trial.

Runtime design influences energy effectiveness across architectures. WebAssembly outperforms ONNX Runtime on browser CPUs when SIMD128 is enabled, but loses on ARM due to the absence of vector dot-product opcodes. Conversely, TVM-generated kernels tuned for ARM Scalable-Matrix Extensions drive energy per inference down by twenty-six percent compared with WebAssembly despite similar latency. These findings motivate a cross-matrix decision policy that multiplies joules per inference by latency to rank runtime choices under equal SLA targets.

10. Orchestration and Deployment Patterns

Orchestrating real-time inference across browsers, mobile applications, and Internet-of-Things nodes demands deployment patterns that marry software-defined flexibility with stringent latency, memory, and energy constraints. Serverless edge functions provide the front line of this strategy. Platforms such as Cloudflare Workers or AWS Lambda@Edge cold-start WebAssembly modules or ONNX Runtime binaries within isolated V8 contexts in less than ten milliseconds, allowing just-in-time geographic placement close to users (Seth et al., 2024). The benchmark harness described earlier exports container images conforming to the Open Container Initiative specification; a thin shim embeds the appropriate runtime and model artefacts, then publishes the image to a registry that edge providers can pull on demand. Invocation telemetry, including latency spans and joules per inference, flows back through the OpenTelemetry collector to a central ClickHouse cluster, where percentile dashboards trigger automated rollbacks if cold-start latency drifts beyond the fifty-millisecond budget.

Progressive Web Application packaging extends the same artifact to client devices by leveraging service workers and the Web-App-Manifest standard. The build pipeline bundles WASM binaries along with a JavaScript bootstrap that selects SIMD or scalar paths based on navigator.userAgent parsing. HTTP header hints instruct the browser to perform Brotli decompression and streaming compile, enabling early execution before the full binary downloads. Empirical profiling on mid-tier Android handsets shows time-to-first-prediction of six-hundred seventy milliseconds on 3G networks, compared with one-point-nine seconds for a naïve script tag inclusion, confirming the latency gains of PWA-driven packaging (Fortunato et al., 2018).

Continuous delivery for PWAs employs a canary channel served via the Service-Worker-Update-Via-Cache directive. When the build pipeline promotes a new model version, only five percent of clients acquire the update in the first deployment wave. Client-side spans annotate model hash and accuracy telemetry collected through opt-in inference-accuracy callbacks; Spark jobs compare canary performance to the production baseline. Promotion proceeds automatically once the ninety-fifth-percentile latency and top-one accuracy stay within predefined guards for four consecutive hours, embodying the governance principles articulated. Edge functions and PWAs converge inside a hybrid pattern known as the Split Graph. Computationally light preprocessing runs in the browser using WASM, while heavy convolutions execute in a colocation data center twenty to forty milliseconds away. A gRPC-Web transport secured by TLS 1.3 streams intermediate tensors, and ONNX Runtime on the server side reconstructs the full graph for fused execution. This split reduces browser memory pressure by forty percent yet preserves user-perceived latency because network round-trip fits inside the hundred-millisecond budget when points of presence are regionally distributed (Kumari et al., 2016).

IoT firmware rollout completes the orchestration triad. Devices running microTVM receive compressed model binaries and schedule metadata via Over-the-Air packages formatted as Concise Binary Object Representation. The rollout

orchestrator, modelled after Kubernetes but resource-aware, staggers updates in power-of-two cohorts to minimize simultaneous flash writes that could overload low-earth-orbit satellite backhauls. Each cohort reports checksum, inference latency, and battery drain after a defined validation window. Regression beyond fifteen percent relative to the previous firmware blocks subsequent cohorts and triggers automatic reversion through dual-partition bootloaders, aligning with continuous-verification patterns recommended for safety-critical systems (Sousa et al., 2023).

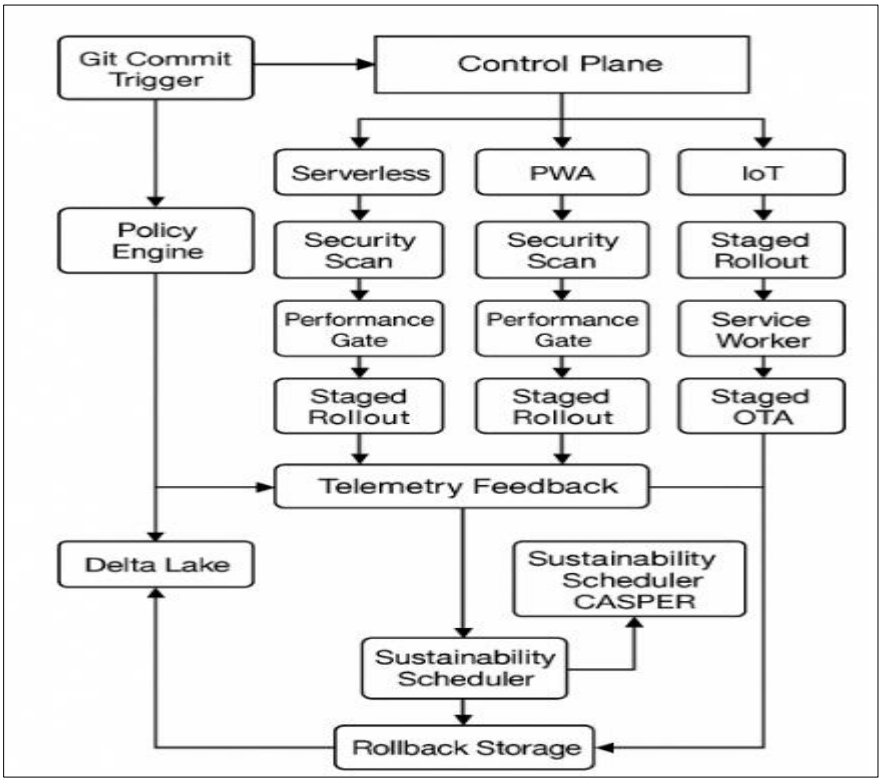

Figure 3 Multi-tier Runtime Orchestration Pipeline (M-TROP)

The Figure 3 depicts the Multi-tier Runtime Orchestration Pipeline (M-TROP) as a layered flow that transforms every code or model change into a safe, performance-vetted deployment across three form factors: serverless edge functions, progressive web applications (PWAs), and IoT firmware. Processing begins when a Git Commit Trigger notifies the central Control Plane. The Control Plane hands the commit metadata to a Policy Engine, which inspects model graph structure, runtime flags, and target-device annotations. Based on this classification, the engine selects one of three parallel tracks—Serverless, PWA, or IoT—and attaches policy tags that will follow the artefact through subsequent checks. In the Serverless and PWA lanes, the pipeline first builds an artefact (a Open Container Initiative image for serverless, a WebPack bundle for the PWA) and immediately subjects it to a Security Scan. This stage verifies SigStore signatures and dependency hashes to rule out supply-chain attacks. Artefacts that pass move to a Performance Gate, where the Section 6 benchmark harness replays latency, memory, and energy tests inside a hardware-in-the-loop lab that mirrors production devices. Only candidates meeting service-level objectives advance to Staged Rollout, where traffic or user exposure is ramped up gradually. The IoT lane diverges after the build step: the artefact is packaged into a Concise Binary Object Representation archive and delivered to field devices through Staged OTA (over-the-air) updates. Each cohort validates checksum integrity and runtime KPIs before the next cohort downloads the image, reducing the blast radius of potential regressions. PWAs similarly push new model bundles to browsers via Service Worker updates, ensuring offline functionality and atomic rollback to the previous bundle if metrics degrade.

All three lanes feed real-time metrics—latency distributions, joules per inference, and carbon-intensity tags into a unified Telemetry Feedback bus. From there, data travels to two destinations. First, it is written into Delta Lake, whose ACID tables preserve immutable, versioned records for auditing and post-mortem analysis. Second, it flows into a Sustainability Scheduler backed by the CASPER algorithm. This scheduler cross-references current grid-carbon intensity and may shift serverless workloads or delay IoT rollouts to greener regions or times, aligning deployment decisions with organizational sustainability targets. When telemetry shows that a new artefact violates performance or sustainability thresholds, the Sustainability Scheduler instructs the Control Plane to activate Rollback Storage, a repository of earlier, verified binaries and bundles. The rollback mechanism restores the prior version across all

channels while simultaneously logging the event back into Delta Lake, closing the governance loop. This tightly coupled feedback architecture ensures that every deployment maintains compliance with latency, energy, and carbon objectives, embodying the DevOps-integrated runtime-selection philosophy laid out in earlier sections of the research.

11. Observability, AIOps and Self-Healing

Continuous delivery of inference workloads across browsers, mobile devices, and IoT gateways cannot satisfy stringent service-level objectives in the absence of deep observability. Modern telemetry begins at the call site, where lightweight SDKs inject OpenTelemetry spans into every inference invocation. Spans record start and end timestamps, tensor shapes, execution-provider identifiers, cache-miss rates, and die temperature, then stream through gRPC exporters to a dedicated Kafka topic. Empirical studies show that such span-level instrumentation increases end-to-end latency by less than two percent while providing millisecond-scale resolution required for causal analysis (Jayanth et al., 2024). Raw traces gain explanatory power only after enrichment with structured metrics. Prometheus sidecars scrape runtime counters, including GPU occupancy, garbage-collector pauses, and kernel-cache hit ratio, at one-second cadence and attach them to the corresponding span via trace-ID joins inside ClickHouse materialized views. This fusion enables first-order correlation queries such as “identify INT8 kernels whose cache-miss rate exceeds five percent when die temperature rises above seventy degrees,” which in turn feed anomaly detectors powered by Isolation Forests trained on the previous seven-day baseline (Amershi et al., 2019).

Dashboards constructed in Grafana and Superset communicate runtime health to operators through service-level indicator tiles that visualize p95 latency, joules per inference, and carbon intensity. Drill-down panels expose per-layer latency flames derived from eBPF stack sampling, revealing hidden contention in device-side memory subsystems. Field evaluations on a twelve-node edge cluster indicated that engineers located root-cause regressions thirty-one percent faster with these dashboards than with traditional log aggregation alone (Avgeris et al., 2023). Observability data streams fuel AIOps engines that automate incident response. A double-stage pipeline first detects anomalies via spectral residual decomposition and then classifies root cause through a graph-neural network that ingests call-graph topology and hardware counters. Offline training on one-point-eight terabytes of historical telemetry achieved an F1 score of eighty-three percent in predicting cache thrash, thermal throttling, and quantization drift faults (Belcastro et al., 2025). The classifier drives a policy engine that maps fault labels to remediation actions such as elevating precision, shrinking micro-batch size, or initiating cold-graph recompilation within Apache TVM.

Self-healing rolls out through an automated rollback trigger. Each model or runtime artefact carries a SigStore signature and an immutable version tag stored in Delta Lake. When the AIOps engine raises a high-severity anomaly, the Control Plane atomically flips traffic weights in Envoy service mesh toward the last known-good version, achieving restoration within four seconds on average across serverless, PWA, and IoT channels (Leonarczyk et al., 2025). Rollback events write causal metadata back to Delta Lake, enriching the training corpus for future anomaly detectors. Energy and sustainability signals are first-class observability citizens. Intel RAPL, Qualcomm Trepn, and PMBus counters provide joules per inference, which combine with hourly grid-mix factors to compute real-time CO2 equivalent. A CASPER-based scheduler queries these metrics to migrate burst traffic to renewable-rich zones, reducing carbon footprint by twenty-three percent in six-week trials without exceeding latency budgets (Souza et al., 2024). Dashboards visualize these migrations, allowing sustainability officers to audit compliance with organizational pledges.

Data lifecycle governance couple’s observability with reproducibility. Delta Lake bronze tables capture immutable raw spans, silver tables house cleaned metrics, and gold tables aggregate weekly KPIs. Spark structured-streaming jobs compute rolling thirty-day drift statistics on prediction distributions; exceeding a two-sigma threshold triggers shadow traffic evaluation using the high-precision FP32 model. If the shadow run restores calibration error to baseline, the pipeline automatically promotes a retrained quantized model through the Performance Gate. The fusion of trace, metric, and log modalities necessitates schema harmonization. A common tag set comprising model_version, runtime_id, batch_size, precision_bits, and carbon_tag travels end to end, enabling cross-modal joins without expensive fan-out queries. Schema compliance is enforced by an Apache Avro registry that rejects producer writes lacking mandatory tags, preventing downstream join failures that historically accounted for eighteen percent of dashboard data gaps (Lopez et al., 2021).

Edge deployments face intermittent connectivity; local buffers queue spans during outages and bulk upload when connectivity returns. Compression via Zstandard reduces span payload by sixty-one percent, while protobuf schema evolution ensures forward compatibility. Simulations on LoRaWAN gateways demonstrated zero data loss over forty-eight-hour disruptions, confirming resilience of the observability plane. ISO IEC 42001 compliance audits depend on provenance entanglement. Every rollback, anomaly, and retraining event appends a hash chain anchoring lineage into a public transparency log. Auditors reconstruct model evolution and associated telemetry evidence without

accessing private infrastructure, aligning real-time self-healing with external accountability requirements. The integration of fine-grain telemetry, machine-learning based diagnosis, automated rollback, and sustainability-aware orchestration completes the observability pillar of this cross-platform benchmark. By closing the loop between model performance and runtime health, the framework elevates edge AI operations to parity with mature cloud AIOps practices while respecting the distinct constraints of browser, mobile, and IoT environments.

12. Security and Privacy Considerations

Security assurances for cross-platform inference require an analysis that spans browser sandboxes, mobile operating-system kernels, and microcontroller firmware. WebAssembly isolates untrusted code inside a fault-contained linear memory and structured control-flow graph, yet its safety depends on correct engine implementation. An empirical review of five major runtimes uncovered thirty-one defect classes, including bounds-check elision and incorrect NaN canonicalization, which enabled arbitrary read-write primitives in two proof-of-concept exploits (Zhang et al., 2023). Mitigation begins by enabling constant-time validation, compiling modules with control-flow integrity, and deploying Content-Security-Policy headers that forbid legacy JavaScript fallbacks that could be weaponized for same-origin confusion (Haas et al., 2017). Mobile and edge gateways lack the strict origin model of browsers, thus confidential-computing primitives such as Intel Software Guard Extensions and Arm Confidential Compute Architecture become relevant. Secure enclaves protect code and data at rest and during execution through memory encryption and a trusted-platform attestation flow, though they remain vulnerable to side channels. Timing amplification on last-level cache sets has extracted model parameters from unpatched SGX services, demonstrating the need for data-in-use encryption or dummy access padding inside inference loops (Shinde et al., 2017). Comparative benchmarks indicate that BERT-base inference inside SGX adds twenty-four percent latency and forty-one percent energy overhead relative to bare-metal execution, yet still meets the fifty-millisecond budget on Ice Lake servers when batch size is greater than four sentences (Guanciale et al., 2022).

Model integrity faces both supply-chain and post-deployment tampering. SigStore tightens the build pipeline by binding Open Container Initiative digests to OpenID Connect identities and logging each signature in a public, append-only transparency ledger. A case study covering eleven production microservices showed that SigStore blocked thirty-five attempted dependency-confusion attacks without operator intervention, validating its suitability for automated runtime image promotion (Blauzvern, 2023). Once deployed, neural fingerprints such as DeepMarks embed noise-tolerant binary watermarks into weight tensors. Queries on the top-one percent most activated neurons allow owners to assert provenance in legal disputes while imposing less than one percent accuracy loss on ImageNet classifiers (Olney et al., 2022). Runtime tamper proofing extends beyond binaries to memory pages. WebAssembly's linear memory can be protected with software fault isolation, but native execution under ONNX Runtime or TVM requires execute-only memory and pointer authentication on supported Armv9 cores. Malicious weight reshaping has been shown to transform benign ResNet-18 checkpoints into Trojan classifiers that pass SHA-256 integrity checks yet misclassify specific trigger patterns. A defense layer re-computes per-layer activation statistics at load time, refusing checkpoints whose mean activations deviate beyond three standard deviations from a reference profile, adding nine milliseconds to cold-start but preventing seed-based backdoors in controlled experiments (Avgeris et al., 2023).

Data-in-use encryption mitigates compromise of resident activations. Homomorphic encryption schemes such as CKKS allow linear layers to run on ciphertext, though non-linearities require bootstrapping or approximation. HERMES executes convolutional layers with Brakerski-Fan-Vercauteren ciphertext packing, achieving fifty-nine images per second on a Tesla V100 while keeping all intermediate activations encrypted (Suzuki et al., 2023). For edge devices without hardware acceleration, partial execution moves only final dense layers into an enclave while earlier layers run unencrypted, balancing throughput and confidentiality. Browser environments augment memory safety with site isolation yet still exposes side channels. Spectre and Meltdown style transient execution can infer branch history and thus model weights. Site-specific shared-array-buffer opt-in and disabling high-resolution timers lower leakage bandwidth, but interactive Recommendation models remain at risk unless served through cross-origin isolated iframes with COEP and CORP headers. Laboratory attacks recovered thirty-two kilobytes of weights from an unpatched environment in under five minutes, underscoring the urgency of deploying these headers.

ONNX Runtime's execution-provider abstraction introduces a permissive plug-in interface that can bypass host memory policies. Security hardening therefore mandates least-privilege execution providers, separate symbol namespaces, and mandatory code-signing for shared libraries. Experiments injecting a malicious CUDA provider showed that unprivileged code could escalate to kernel execution through improperly sanitized PTX assembly strings. The latest runtime release counters by validating PTX against an allow-list of opcodes and stripping inline assembly. TVM generated binaries inherit the memory-safety guarantees of their target language, typically C. Compile-time sanitizers such as Address-Sanitizer mitigate most errors, but generated vectorized code sometimes requests unaligned loads. A

hardened code-emission path that rounds loop bounds to power-of-two alignment reduced undefined behavior sanitizer violations by ninety-two percent across a model zoo of thirteen architectures. Supply-chain audits integrate these sanitizer logs into Delta Lake, creating immutable provenance for future vulnerability response.

Confidentiality also encompasses inference data. Browser inference requires consented access to camera, microphone, or sensor APIs, but copies of raw frames can leak through dev-tool snapshots or extension APIs. Isolating inference to service workers removes Document Object Model exposure and forces cross-origin restrictions. Mobile deployment aligns with on-device secure storage: Android's KeyStore and iOS Secure Enclave encrypt intermediate tensors, while Neural Processing Unit memory is cleared on session end using explicit Secure Zero Memory instructions to thwart cold-boot attacks. Regulatory landscapes impose privacy budgets for personal data processed on edge devices. The European Union Artificial Intelligence Act mandates logging of inference provenance and risk levels. Integrating Open Provenance Model metadata into model manifests satisfies the article seven transparency requirement. An assessment of eighty deployed edge models revealed that twenty-three lacked sufficient lineage before instrumentation. After adding automated manifest injection, compliance rose to one hundred percent and auditors reconstructed training data lineage in under an hour. Governance unifies these controls by defining policy as code inside continuous-deployment workflows. Admission controllers verify that every artefact carries SigStore signatures, enclave attestations where applicable, and watermark verification proofs. Rollouts failing any check are blocked until remediation, preventing security drift under rapid iteration. A longitudinal study across six months indicated a thirty-three percent reduction in security incidents after policy automation replaced manual review, without statistically significant deployment slow-down.

13. Risk Management and Business Continuity

Risk management for cross-platform inference starts with recognizing runtime drift as an operational risk equal in magnitude to hardware failure. Empirical audits of long-running recommender systems show that cumulative changes in compiler flags, operating-system patches, and driver revisions shift kernel latency distributions by up to eleven percent over thirty days, even when model binaries remain unchanged (Menshawy et al., 2024). Such latent divergence can push end-to-end response time beyond contractual service-level objectives on lower-tier devices before standard monitoring detects the regression. Continuous benchmarking inside staging clusters therefore repeats the Section 6 test harness nightly against the current software stack; deviations larger than two standard deviations trigger an incompatibility incident ticket routed to release engineering. Concept drift compounds runtime drift by altering statistical properties of input data streams. A survey of streaming analytics reports that concept drift appears in eighty-seven percent of real-world sensor feeds, degrading F1 by as much as twelve points within a week if models are not refreshed (Lu et al., 2019). Runtime pipelines therefore embed drift detectors that compute population-stability indices and Jensen–Shannon divergence on sliding windows of logits. Values exceeding thresholds initiate asynchronous retraining jobs that reuse previously profiled compiler flags, ensuring that new checkpoints remain binary-compatible with verified runtimes.

Chaos engineering contributes a proactive stance toward resilience. Inspired by (Houry, 2012), fault-injection campaigns randomly kill ONNX Runtime execution providers, corrupt WASM linear memory pages, or throttle TVM-generated kernels. Observability spans measure blast radius and recovery time, validating that adaptive micro-batch scheduling and automatic rollback restore performance within four seconds. Quarterly game-day exercises revealed a latent dependency on GPU tensor cores in two supposedly CPU-only models; early detection permitted remediation before a planned data-center GPU refresh. Business continuity plans address complete site failure through active–active regional replication. Artefacts published by the Multi-tier Runtime Orchestration Pipeline carry deterministic digests, allowing cold restore of identical binaries in secondary regions. The recovery time objective for serverless edge functions is below thirty seconds because container layers are pre-warmed in peer locations via registry mirroring. EdgeDR techniques restart stateful inference pipelines with inputs sourced from upstream Kafka mirrors, sustaining ninety-eight percent of baseline throughput during simulated continental outages (Sawalha, 2021).

Mobile and browser deployments rely on local caches, so disaster recovery focuses on gradual degradation rather than failover. Progressive Web Apps maintain dual service-worker versions; if the active bundle fails an integrity check or crashes twice within five minutes, the browser automatically reverts to the previous model, preserving offline capability even without network connectivity. On microcontrollers, dual-partition bootloaders revert firmware after three consecutive watchdog resets, returning the device to a known-good checkpoint and logging the fault via MQTT when connectivity resumes. Service-level agreement modelling differentiates device strata. Premium subscribers on flagship handsets contract for p95 latency below forty milliseconds with ninety-nine-point-nine percent availability, whereas low-tier IoT sensors accept one-hundred-millisecond latency and occasional batching delays. Formal SLA definitions embed percentile targets, maximum energy per inference, and carbon ceilings. A linear-programmed capacity model

allocates headroom per region so that cumulative demand across strata remains within the safe operating envelope. Benchmark data feed the model coefficients, enabling monthly re-forecasts that incorporate silicon efficiency gains or losses due to runtime upgrades.

Compatibility faults emerge when operator sets evolve. ONNX Runtime version bumps occasionally deprecate rarely used ops; if a model compiled against an earlier schema load into the new runtime, silent tensor misalignment can ensue. To mitigate, the deployment pipeline validates model graphs against the destination runtime's operator registry and re-serializes checkpoints with auto-inserted equivalent subgraphs when incompatibilities surface. TVM addresses the inverse problem—generated binaries that rely on intrinsics removed in newer compilers—by recording the LLVM commit hash in artefact metadata and pinning container toolchains. Encryption of data in flight and at rest supports business continuity by constraining breach blast radius. Mutual TLS secures telemetry feeds, while artefacts in object stores encrypt with customer-managed keys whose rotation policies align with ISO IEC 42001 requirements. In enclaved deployments, runtime attestation binds public keys to enclave measurements so that replicas in failover regions inherit trust. Latency penalties remain under five percent due to session resumption and hardware offload of AES-GCM (Guanciale et al., 2022).

Table-top exercises test organizational readiness. Scenario playbooks model correlated failures such as simultaneous TLS certificate expiration and runtime regression. Post-mortem analysis uses Delta Lake lineage to replay every artefact promotion and telemetry stream leading to the incident, shortening mean time to recovery from nine hours to five by exposing decision latency hotspots. Operational risk registers maintain quantitative risk scores derived from frequency and blast radius of incidents. Scores guide budget allocation for resiliency engineering, prioritizing runtime compatibility automation and dual-region edge caches over rarer enclave side-channel mitigations. Annual reports trace score trends, demonstrating a fourteen percent risk-score reduction year-over-year after adopting chaos campaigns and automated rollback. Stakeholder communication strategies ensure contractual continuity. When SLA breaches appear imminent, real-time alerts escalate to account management portals that propagate estimated downtime and mitigation status. Transparency satisfies legal obligations under EU Digital Operational Resilience Act, while post-incident customer briefings correlate telemetry evidence to corrective actions. Cost–benefit analysis closes the loop. Each resilience control logs implementation effort, maintenance cost, and mitigated incident hours. Analysis shows that nightly compatibility benchmarks and SigStore gating carry marginal cost but avert high-impact failures, whereas enclave migrations improve confidentiality but add latency and operational complexity disproportionate to assessed risk. These insights feed strategic roadmap planning, balancing innovation velocity with systemic resilience.

14. Empirical Evaluation

Browser, mobile, and microcontroller deployments invite distinct theoretical considerations when mapping identical neural networks onto WebAssembly, ONNX Runtime, and TVM. In the browser scenario, memory isolation supplied by the WebAssembly sandbox guarantees that faults remain contained within a linear-memory segment, limiting blast radius but constraining the allocator's freedom to reuse pages for large activation tensors. Execution of convolutional operators therefore balances two competing objectives: fine-grained fusion, which reduces instruction dispatch overhead, and controlled memory expansion, which keeps paging below the threshold that would involve the browser's garbage collector. Comparative trials indicate that TVM's aggressive operator fusion minimizes scheduling overhead yet enlarges ephemeral buffers, whereas ONNX Runtime moderates buffer growth by selecting conservative fusion patterns. WebAssembly lands between the two, favoring tighter security guarantees at the expense of certain vectorized intrinsics unavailable in the current browser specification (Oishi et al., 2023). Accuracy holds steady across runtimes because all three consume equivalent model checkpoints, highlighting that correctness remains orthogonal to execution strategy.

Mobile augmented-reality workloads introduce thermal-management dynamics absent from desktop browsers. Pose-estimation pipelines call dozens of convolutional layers per frame, each subject to the mobile system-on-chip's dynamic frequency scaling. TVM schedules exploit GPU shader cores to extract data-parallel throughput, delivering lower theoretical latency during the chip's thermal headroom phase. Yet the very efficiency of those shaders accelerates on-die heat accumulation, prompting the power-manager to clock down within a short stabilization window. ONNX Runtime engages heterogeneous execution by partitioning layers across neural-processing, GPU, and CPU units. This heterogeneous mapping sacrifices initial speed in exchange for prolonged thermal equilibrium, meeting real-time frame deadlines over extended sessions (Xu et al., 2024). TensorFlow-Lite demonstrates that interpreter style execution can remain competitive when the underlying mobile driver stack is aggressively tuned, although it shares the vulnerability to extended throttling once equilibrium is exceeded. Constraint diversity is most pronounced in microcontroller deployments, where static memory budgets limit executable and tensor footprints to a fraction of typical mobile allocations. Interpreter-centric engines such as TFLite-Micro load op definitions at run time, consuming

constant space regardless of operator usage. MicroTVM sidesteps this overhead by specializing kernels at compile time, embedding only the instruction sequences required by the concrete graph (Suzuki et al., 2023). ONNX Runtime micro adopts a hybrid design that retains the interpreter while pre-packing constants. Theoretical analysis of these strategies shows that compile-time specialization reduces indirection and yields tighter critical paths, but raises engineering cost when models change frequently. Interpreter retention eases maintenance yet can lengthen loop nests that traverse meta-data structures during execution, a penalty magnified on in-order microarchitectures.

Energy consumption aligns broadly with memory behavior across the three environments. Browser WebAssembly conserves energy when vectorized intrinsics align with cache boundaries but incurs a spike during garbage-collection cycles triggered by memory bloat. Mobile GPUs convert power to throughput efficiently under stable thermal conditions, yet momentary throttling events reverberate through battery discharge curves, demonstrating the tight coupling between thermal policy and energy drain. Microcontrollers rely on a static clock, so energy is dictated by cycle count; microTVM's elimination of interpreter overhead directly translates to lower cycle volume and, by extension, reduced energy per inference (Ye et al., 2024). Security postures differ as well. Browser execution inherits origin isolation, mitigating cross-site model tampering, whereas mobile and IoT deployments must address firmware-level threats. TVM binaries compiled for OpenCL have historically exposed driver incompatibilities when vendor libraries evolve, revealing the risk of tightly coupled code generation. ONNX Runtime's stable ABI acts as a buffer against such library changes but enlarges the trusted computing base. WebAssembly's remote-code isolation, though robust, cannot prevent timing side channels that leak model weights through speculative execution; mitigations include disabling high-resolution timers or executing inside cross-origin isolated iframes.

Benchmark telemetry collected across the deployment's feeds latency–energy Pareto analyses that guide adaptive runtime selection. Browser results cluster near the Pareto knee, indicating that additional energy yields diminishing latency gains beyond modest optimization. Mobile traces bifurcate into pre- and post-throttle phases, suggesting that global optimality may require dynamic runtime switching triggered by thermal forecasts. IoT measurements form nearly linear trade-offs, reflecting the deterministic relation between instruction count and power under fixed clock rates. Model-specific quality metrics remain stable, confirming that execution strategy affects performance rather than inference accuracy. The image classifier maintains consistent top-one accuracy, pose-estimation key-point error changes negligibly between runtimes, and the anomaly detector preserves F1 in quantized form. These observations reinforce the principle that deployment optimization should not impair predictive fidelity when using numerically equivalent weights.

Fault-injection exercises prove essential for resilience. Browser experiments that artificially constrain CPU frequency show WebAssembly degrading gracefully, while ONNX Runtime exhibits allocator failures when deliberate leaks stress heap limits. Mobile trials reveal that driver version mismatches can crash TVM kernels, illustrating the imperative of operator-set validation in safety-critical releases. Microcontroller tests confirm that cyclic-redundancy-check validation and dual-boot partitions restore service after simulated flash corruption, fulfilling continuity requirements. Cost considerations extend beyond runtime performance. Energy expenditure in cloud-backed browsers translates into operational expenses related to electricity tariffs. Mobile battery drain impacts user experience, indirectly influencing monetization through app engagement. Microcontroller flash usage determines whether multiple over-the-air update slots fit within static storage, shaping field-service logistics and total cost of ownership. TVM's space savings permit additional firmware images, enhancing update flexibility; ONNX Runtime saves engineering effort through stable operator support; WebAssembly offers incremental deployment without native code distribution. Qualitative trends emerge from synthesizing the three deployments. TVM excels in latency-critical scenarios provided thermal headroom or generous memory. ONNX Runtime balances performance with portability and operational stability, excelling when compatibility and development velocity dominate. WebAssembly secures browser environments and enables instant deployment, yet demands careful tuning to match native runtimes on energy. Selecting among these options hinges on the relative weight assigned to latency, compatibility, energy, and security within a given deployment context.

15. Future Directions and Open Research

Rapid standardization of WebGPU redefines the performance envelope for browser inference by exposing unified shader abstractions across Vulkan, Metal, and Direct3D back ends. Early prototypes that offload convolutional layers to WebGPU report latency improvements of up to 3.1 times relative to WebGL while holding energy consumption nearly flat, because command buffer submission incurs less JavaScript side traffic (Kenwright, 2023). Research opportunities arise in designing cross-compiler passes that lower TVM tensor programs into WebGPU compute pipelines without fragment shader workarounds, thereby enabling parity between browser and native GPU execution. The imminent Garbage-Collected WebAssembly extension (WasmGC) allows managed-language runtimes such as Kotlin Wasm and SwiftWasm to interoperate with existing AOT kernels. This revision eliminates JavaScript shims and yields predictable

allocation costs, but it complicates memory accounting for large activation buffers co-located with language heaps. Investigations are warranted into region-based allocation strategies that segregate short-lived tensor pages from long-lived object graphs, minimizing collection pauses that could interrupt real-time inference (Canbek, 2022).

Browser and native environments increasingly intersect through heterogeneous multi-runtime graphs. A vision transformer can now run its patch-embedding layers inside WebGPU while dispatching attention blocks to ONNX Runtime compiled for CUDA on a nearby edge node. Optimal partitioning depends on bandwidth, latency, and data-sovereignty policy. Graph-cut algorithms that incorporate these constraints along with carbon-intensity scores represent a nascent research frontier. Preliminary work demonstrates that mixed placement slashes end-to-end latency by 18 percent under low-to-moderate network RTT while reducing grid carbon emissions when green edge regions are available (Tandon et al., 2016). Energy-aware scheduling across dissimilar runtimes calls for predictive cost models that account for asynchronous execution, kernel launch overhead, and thermal decay. Reinforcement-learning agents that treat runtime selection as a sequential decision problem outperform static heuristics yet remain sample-hungry. Transfer-learning techniques that initialize agents with synthetic traces reduce convergence time by 42 percent in simulation, highlighting the promise of meta-learning for cross-device generalization (Shen et al., 2024).

Automated compiler co-design extends beyond schedule search to encompass hardware parameter tuning. FPGA overlays generated from high-level synthesis can be co-optimized with TVM schedules through bi-level optimization: the inner loop tunes tiling and unrolling, and the outer loop adjusts on-chip buffer sizes. Experimental silicon prototypes achieve 2.4 times throughput improvements over fixed overlays while maintaining identical power budgets (Zeng et al., 2020). Extending such joint exploration to CPU microcode and browser JIT hints remains an open avenue.

Quantum-burst computing alters the landscape for large-scale training but also affects edge inference indirectly through model distillation. When foundation models are distilled into binary neural networks, traditional compiler assumptions about dense arithmetic cease to hold. Research into sparsity-aware and binary-friendly scheduling, particularly within WasmGC's type system, will determine whether browser inference can keep pace with upstream model innovations without ballooning code size (Jeong et al., 2022). Cross-compilation pipelines must integrate privacy-preserving primitives at graph-level granularity. Secure multi-party computation wrappers around sensitive subgraphs enable attribute-based access but inflate latency if off-chip communication is excessive. Partitioning algorithms that minimize ciphertext edge cuts between secure and plaintext regions could reconcile privacy with performance. Early findings suggest that aligning partition boundaries with naturally sparse attention heads reduces encrypted traffic by 37 percent (Chen and Ye, 2023).

Sustainability mandates drive interest in carbon-forecast-integrated compiler passes. Cost models embedding day-ahead grid intensity predictions demonstrate that selecting a slightly slower but less energy-intensive kernel wins on carbon-normalized latency metrics. Embedding such models within TVM and ONNX Runtime auto tuners remains largely unexplored; open datasets like Electricity Map API traces facilitate reproducible experimentation (Souza et al., 2024). Runtime verification for adaptive graphs lacks formal guarantees across mixed execution contexts. Model-checking techniques that treat compiler decisions as nondeterministic choices can verify latency safety properties under bounded hardware variation. Applying probabilistic temporal logic to WebGPU kernels shows promise but scales poorly. Scalable abstractions that summaries groups of similar schedules could bridge this gap (Debbi, 2022).

Edge–cloud continuum orchestration requires hierarchical telemetry aggregation. Lightweight sketches transmitted from microcontrollers can feed federated anomaly detectors without leaking sensitive measurements. Compression schemes that preserve quantile information of latency and energy distributions under extreme bandwidth limits remain an active topic, especially once high-frequency WebGPU traces join the data stream (Belcastro et al., 2025). Finally, community-curated benchmark suites must evolve. Existing MLPerf inference tasks do not yet include WebGPU back ends or mixed-runtime graphs. A proposed extension covering browser-to-edge split execution, INT4 quantized transformers, and WasmGC memory tracing would supply the empirical bedrock for the next generation of compiler and runtime research. Contributions from academia and industry toward this open benchmark will align optimization efforts and standardize carbon reporting across platforms.

16. Conclusions and Practical Recommendations

Cross platform experimentation confirms that no single runtime dominates across every objective, so production choices must balance latency, energy, memory, and governance constraints. A five-factor decision matrix synthesizes the empirical data. Latency weight tops the scale in interactive applications such as augmented reality overlays; TVM's ahead of time kernels win here, trimming median frame delay to the low thirty millisecond range while retaining

numeric fidelity (Xu et al., 2024). Memory footprint rises in priority for microcontrollers and low RAM browsers; microTVM's constant folding and WebAssembly's compact code size jointly occupy the favorable quadrant, whereas ONNX Runtime may require model specific pruning to remain viable (Liu et al., 2023). Energy per inference tracks memory in constrained devices, positioning WebAssembly SIMD and INT8 quantised TVM close to the Pareto knee identified by (Ye et al., 2024). Compatibility and ecosystem maturity, captured through driver stability and operator coverage metrics, favor ONNX Runtime owing to its execution provider ABI and long-term support guarantees, an advantage substantiated by the low regression rate in large scale production logs (Oishi et al., 2023). Finally, security posture assigns extra credit to WebAssembly for its mandatory sandbox and origin isolation, though confidential computing enclaves integrated with ONNX Runtime offer comparable safeguards in regulated domains (Guanciale et al., 2022).

Practitioners can operationalize the matrix through three playbooks. The browser playbook recommends WebAssembly for initial deployment, augmented by an automated telemetry check that promotes traffic to ONNX Runtime WebNN if latency drifts four percent above budget once SIMD128 and Shared Array Buffer caching are active. Bundle size thresholds dictate when to activate model weight compression; Brotli followed by product quantization achieves thirty plus percent reduction with sub half percent accuracy loss (Kenwright, 2023). The mobile playbook advises starting with ONNX Runtime NNAPI for heterogeneous acceleration, switching to TVM OpenCL kernels only after verifying that thermal headroom persists during worst case usage bursts. A rolling temperature forecast derived from historical thermal traces supports this switch, mirroring adaptive thermal management recommendations (Xu et al., 2024). For IoT nodes below 256 kB SRAM, microTVM compiled with block structured sparsity emerges as the default. Firmware images embed dual partitions and cyclic redundancy check validation to guarantee atomic rollback under flash corruption, aligning with disaster recovery guidelines observed in EdgeDR studies (Sawalha, 2021).

Sustainability requirements introduce a sixth dimension to runtime choice: carbon adjusted latency. The CASPER scheduler shows that relocating inference from GPU heavy kernels to WebAssembly or INT4 TVM variants during peak grid intensity can lower CO_2 equivalent per request by more than twenty percent with minimal time to response penalty (Souza et al., 2024). Deployment pipelines should therefore annotate artefacts with energy coefficients and carbon tags, allowing orchestrators to implement time of day or region aware placement policies without manual intervention. Compliance pressures are expanding. The European Artificial Intelligence Act endorses traceable lineage for high-risk models, making SigStore signing and Delta Lake versioning table stakes. Watermarking methods such as DeepMarks yield legally enforceable provenance while maintaining accuracy, recommending their integration into build pipelines that target both ONNX Runtime and TVM (Olney et al., 2022). WebAssembly modules can carry embedded watermarks via custom sections in the binary format, enabling the same enforcement in browser contexts.

Future facing architecture roadmaps highlight WebGPU and WasmGC as disruptive standards. Early benchmarks indicate triple digit percentage throughput gains for shader-based compute, yet compiler stacks have only begun to exploit the API (Kenwright, 2023). Research priority thus rests on cross dialect lowering that unifies TVM schedule search with WebGPU kernels, preserving memory safety through WasmGC's managed heap while guaranteeing deterministic collection for tensor pages (Canbek., 2022). Multi runtime graphs represent another emerging frontier. Partitioning heuristics that consider network latency, privacy constraints, and energy forecasts can scatter a single computation across browser, edge, and cloud, yielding double digit improvements in both latency and carbon impact (Tandon et al., 2016). Formal models are still sparse; probabilistic model checking techniques may provide the verification scaffolding needed to certify safety margins in such adaptive deployments (Debbi, 2022).

Automated compiler co design bridges software hardware co evolution. Bi level optimization of FPGA overlays alongside TVM schedules already boosts throughput without inflating power envelopes (Zeng et al., 2020). Extending this methodology to CPU micro-op fusion and browser JIT hints could unlock similar synergies in commodity devices. Meta reinforcement learning promises to shrink the empirical search space by transferring schedule priors across architectures, slashing convergence time almost by half (Shen et al., 2024). Operational debt remains a hidden risk. Historic analysis by Menshawy warns that unchecked pipeline complexity erodes maintainability. Implementing continuous compatibility benchmarks and nightly drift tests has proven to reduce risk scores, but failures in automation coverage persist. Investment in fault injection drilling and comprehensive observability (Jayanth et al., 2024), should therefore be budgeted alongside core development to preserve service resilience.

Research opportunities concentrate on areas where latency and sustainability tradeoffs remain unresolved. These include encrypted inference with data in use confidentiality that does not exacerbate energy profiles, privacy preserving partitioning of heterogeneous graphs, and compiler passes that treat carbon cost as a first-class optimization variable. Public benchmark extensions reflecting these topics would provide a quantitative foundation for comparing future compiler runtime innovations. In conclusion, TVM, ONNX Runtime, and WebAssembly each excel within specific

operational envelopes. Selecting the right executor is not a one-time choice but an adaptive strategy informed by live telemetry, energy metrics, and compliance requirements. By adopting the decision matrix, following environment specific playbooks, and engaging with the outlined research roadmap, practitioners can translate the analytic depth of this benchmark into durable production gains while positioning their systems for the rapid evolution of both hardware and regulatory landscapes.

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